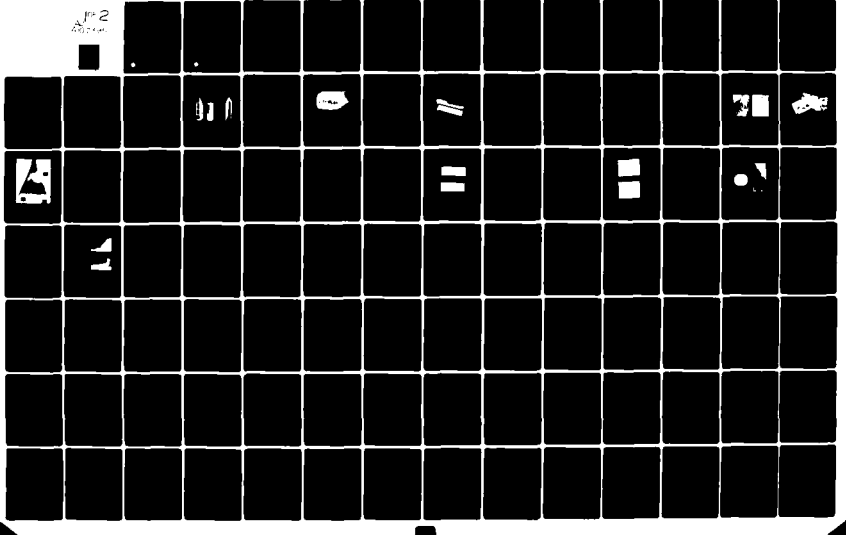
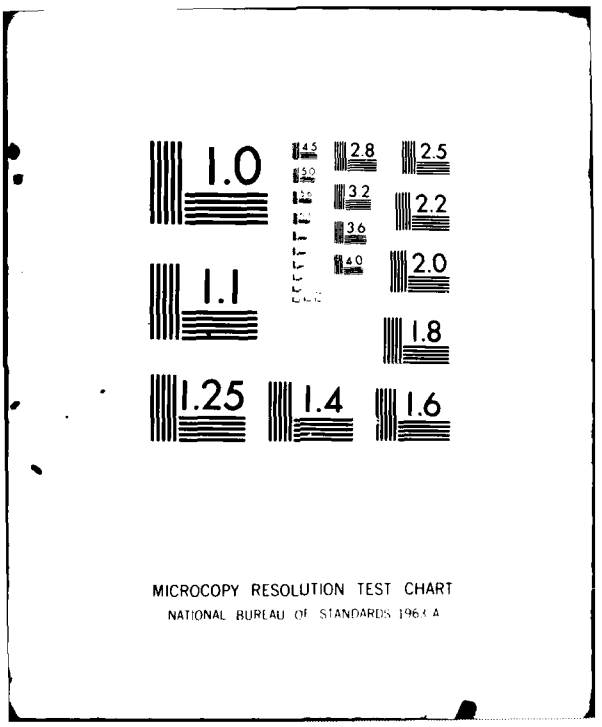
AD-A107 395 WESTINGHOUSE RESEARCH AND DEVELOPMENT CENTER PITTSBU--ETC F/G 20/2
PREPARATION OF LARGE-DIAMETER GAAS CRYSTALS,(U)
SEP 81 H M HOBGOOD, T T BRAGGINS, D L BARRETT N00014-80-C-0445
UNCLASSIFIED 81-9F7-BOULE-R5 NL

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FIRST ANNUAL REPORT

H. M. Hobgood, T. T. Braggins, D. L. Barrett,
G. W. Eldridge and R. N. Thomas

LEVEL II

September 18, 1981

Office of Naval Research/
Defense Advanced Research Projects Agency
Contract No. N00014-80-C-0445

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER	2. GOVT ACCESSION NO. AD-A107 395
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle) Preparation of Large-Diameter GaAs Crystals.	5. TYPE OF REPORT & PERIOD COVERED Annual Report. June 1980-June 1981
	6. PERFORMING ORG. REPORT NUMBER 81-9F7-BOULE-R5
7. AUTHOR(s) H. M./Hobgood, T. T./Braggins, D. L./Barrett, G. W./Eldridge, R. N./Thomas	8. CONTRACT OR GRANT NUMBER(s) N00014-80-C-0445
9. PERFORMING ORGANIZATION NAME AND ADDRESS Westinghouse R&D Center 1310 Beulah Road Pittsburgh, PA 15235	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS PE. 62712E Task # NR 243-030 Project #0Y10
11. CONTROLLING OFFICE NAME AND ADDRESS Office of Naval Research/Defense Advanced Research Projects Agency	12. REPORT DATE September 18, 1981
	13. NUMBER OF PAGES 126
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report)
	15a. DECLASSIFICATION DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

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18. SUPPLEMENTARY NOTES

ONR Scientific Officer 202-696-4218

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

gallium arsenide, crystals, semi-insulators, substrates, encapsulation, growth, crucibles, implantation, large, diameter, defects, reduction, impurity, striation

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Large dia. (50 to 75 mm) semi-insulating LEC GaAs crystals of superior quality have been prepared by in-situ synthesis and pulled from pyrolytic boron nitride (PBN) crucibles, and improved FET channels by direct ion-implantation of these substrates have been achieved. Undoped GaAs/PBN crystals consistently yield: 1) substrate resistivities approaching 10^8 ohm-cm; 2) thermal stability under implantation annealing; 3) lowest concentrations (by SIMS) of active impurities; 4) 6000 cm^2/vsec mobilities corresponding to ionized impurities of $\sim 1 \times 10^{16}$ cm^{-3}; 5) Si implanted power FET channels with ±5% uniformity, 80% activation, 4800-5000 cm^2/vsec mobilities.

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SUMMARY

Significant progress has been made toward developing large-diameter, semi-insulating GaAs crystals of improved quality by LEC growth for direct ion implantation. The intent has been to (1) develop a reproducible twin-free growth technique for large-diameter 50-mm and 75-mm GaAs crystals; (2) achieve stable, semi-insulating substrate properties without resorting to intentional doping with chromium (or at least to reduce the Cr content significantly) to avoid the serious redistribution problems associated with this impurity; (3) obtain uniform, predictable doping characteristics by direct ^{29}Si implantation; and (4) demonstrate that uniform, round cross-section slices suitable for low-cost IC processing can be fabricated from LEC crystals. The specific accomplishments of this work are outlined below.

- Large-diameter (up to 90 mm) <100>-oriented GaAs crystals have been grown by the use of the LEC method. In-situ compounding in pyrolytic boron nitride (PBN) crucibles and very low-moisture content B_2O_3 (assured by vacuum baking) are key ingredients to achieving reproducible semi-insulating <100> crystals of high purity and structural quality.

- Large-diameter GaAs crystals grown from high-purity melts in PBN crucibles contain significantly lower concentrations of electrically active impurities than LEC and boat-grown crystals prepared in fused-silica containers. Mobilities measured on as-grown GaAs/PBN substrates are in the 4500 to 7000 $cm^2/vsec$ range and suggest an ionized impurity density of $\sim 1 \times 10^{16}$ cm^3.

- Consistent, high resistivities ($>10^7$ ohm-cm) and thermally annealed sheet resistivities ($>10^6$ ohm-cm), which have been shown to yield acceptably low leakages and RF losses in analog power circuits, are achieved from only GaAs/PBN-grown crystals and not from GaAs crystals pulled from quartz crucibles.

- Direct ion-implantation studies of undoped and lightly Cr-doped (low 10^{15} cm^{-3} Cr) GaAs/PBN using ^{29}Si implants yield

reproducible implant profiles showing excellent agreement with LSS theoretical predictions.

- Directly implanted channels with the (1 to 1.5) $\times 10^{17}$ cm^{-3} peak donor concentrations required for X-band power FET structures yield electron mobilities between 4800 and 5000 cm^2/vsec.

- Channel dopings down to 2×10^{16} cm^{-3} have been implanted into undoped GaAs/PBN substrates and mobilities of 5700 at 298K and 14,500 cm^2/vsec at 77K have been measured.

- A self-consistent, amphoteric doping behavior is observed for Si implants in undoped GaAs/PBN and Cr-doped GaAs and the total electrical activation ($N_A + N_D$) is 100%.

- Materials preparative techniques such as centerless-grinding and <110> flatting of GaAs boules, as well as edge-rounding of GaAs wafers, have been successfully applied to bulk GaAs crystals to demonstrate the fabrication of uniformly round large-area <100> GaAs wafers, needed to realize a reliable, low-cost GaAs IC manufacturing technology.

1. INTRODUCTION

The present development of monolithic microwave GaAs circuits is based on a selective direct ion implantation of semi-insulating substrates because of its greater flexibility compared with epitaxial techniques for planar device processing. However, direct implantation technology imposes severe demands on the quality of the semi-insulating GaAs, and the unpredictable and often inferior properties of commercially available, horizontal Bridgman and gradient freeze substrates in the past has been a major limitation to attaining uniform and predictable device characteristics by implantation. Problems of substrate reproducibility have been well recognized in a symptomatic sense and have been attributed to excessive and variable concentrations of impurities, particularly silicon and chromium, and with the redistribution of these impurities during implantation and thermal processing. Monolithic GaAs circuits require substrates which: 1) exhibit stable, high resistivities during thermal processing, to maintain both good electrical isolation and low parasitic capacitances associated with active elements; 2) contain very low total concentrations of ionized impurities so that the implanted FET channel mobility is not degraded; and 3) permit fabrication of devices of predictable characteristics so that active and passive elements can be matched in monolithic circuit designs.

Another important consideration is the need for uniformly round, large-area substrates. Broad acceptance of GaAs ICs by the systems community will occur only if a reliable GaAs IC manufacturing technology capable of yielding high-performance monolithic circuits at reasonable costs is realized. Unfortunately, the characteristic D-shaped slices of boat grown GaAs material have been a serious deterrent to the achievement of this goal, since much of the standard semiconductor processing

equipment developed for the silicon IC industry relies on uniformly round substrate slices. Improvements in the basic GaAs materials and its availability as round, large-area substrates are therefore key requirements if a high-yield, low-cost GaAs IC processing technology is to be realized in the near future.

The principal objective to be accomplished in this program is the development of large-diameter, semi-insulating GaAs substrates of high crystalline quality, very high purity, and thermal stability. The underlying aim will be to establish a reliable and reproducible growth technology for preparing high-resistivity substrates of superior quality to realize the full potential of direct ion implantation as a reliable, cost-effective fabrication technology for high-performance GaAs MESFET and integrated circuits.

To address these problems, the growth of high-quality, large-diameter GaAs crystals by the Liquid-Encapsulated Czochralski (LEC) technique and the fabrication technology for producing cassette-compatible, large-area substrates from these circular cross-section crystals has been investigated.

In the liquid-encapsulated Czochralski technique, the dissociation of the volatile As from the GaAs melt, which is contained in a crucible, is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a nonreactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure. In-situ compound synthesis can be carried out from the elemental Ga and As components since the boric oxide melts before significant sublimation starts to take place (~450^{o}C). Compound synthesis occurs rapidly and exothermally at about 820^{o}C under a sufficient inert gas pressure (~60 atm) to prevent sublimation of the arsenic component. Crystal growth is initiated from the stoichiometric melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.

The Melbourn high-pressure LEC puller used in this work is a resistance-heated six-inch diameter crucible system capable of charges

up to 8 to 10 kg weight and can operate at pressures up to 150 atmospheres. The GaAs melt within the pressure vessel can be viewed by means of a closed-circuit TV system. A high-sensitivity weight cell continuously weighs the crystal during growth and provides a differential weight signal for manual diameter control. In addition, a unique diameter control technique which involves growing the crystal through a diameter-defining aperture made of silicon nitride has been developed for <111>-oriented growth. In this "coracle" technique, the defining aperture is fabricated from pressed silicon nitride, which conveniently floats at the GaAs melt/B_2O_3 encapsulant interface.

Using this type of high-pressure LEC puller, crystal purity can be preserved by in-situ elemental compounding[1] and reproducible semi-insulating GaAs achieved by employing silicon-free pyrolytic boron nitride crucible techniques.[2-5] The growth of large-diameter <100>-oriented GaAs crystals, investigations of materials purity and semi-insulating properties and their characterization for directly implanted power IC fabrication are reported in the following sections.

2. CRYSTAL GROWTH STUDIES

The current growth studies have focussed on the development of a reproducible growth methodology for preparing nominally 50- and 75-mm diameter, <100>-oriented GaAs crystals free of major structural defects such as twin planes, lineage, inclusions, and precipitates. In addition, the growth of chromium-free semi-insulating GaAs crystals from melts synthesized in-situ from 6/9s purity Ga and As charges and contained in a pyrolytic boron nitride crucible has been emphasized in these studies. However, GaAs crystals pulled from undoped and chromium-doped melts contained in conventional fused-silica crucibles have also been carried out for comparison of materials properties.

2.1 LEC Growth From Large GaAs Melts

A photograph of a typical 50-mm nominal diameter, <100> semi-insulating GaAs crystal grown from a 3-Kg charge is shown in Fig. 1(a). The use of very clean conditions during crucible loading and growth, vacuum baking of the boric oxide encapsulant to assure a water-free oxide, and a growth technique to produce crystals with sharp cone angles during the initial stages of growth were found to be essential ingredients to achieving twin-free <100> growths.

The growth of crystals in the <100> orientation has relied upon the ability to control nominally the crystal diameter by continuously monitoring the crystal weight and the instantaneous derivative of the weight gain signal (DWS). On the basis of these measured quantities plus visual monitoring through the TV system, adjustments to the power level are made to correct for undesirable changes in crystal diameter.

Owing to reliance upon operator judgment and the inability to see clearly the growth miniscus through the oxide layer, as well as

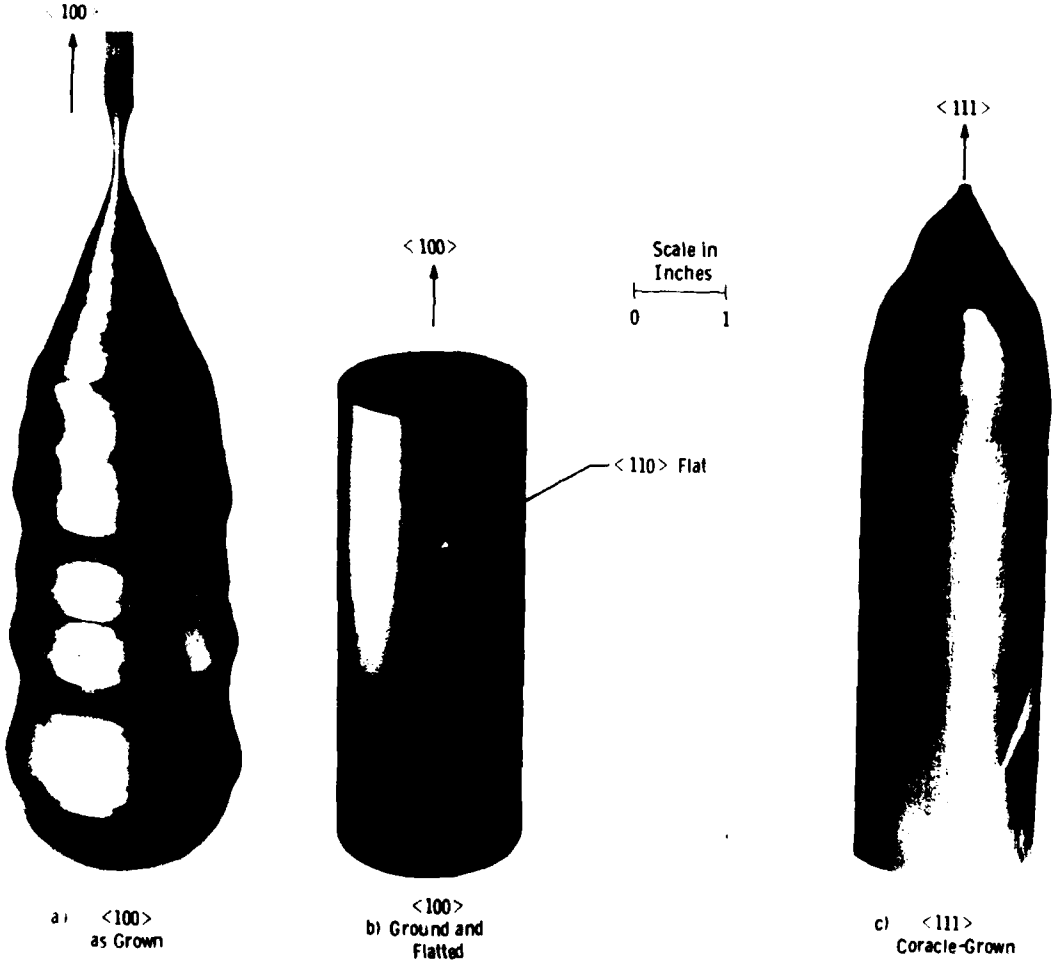

Figure 1 Photograph illustrating: (a) as-grown, nominally 2-inch dia., semi-insulating, <100> GaAs crystal; (b) <100> GaAs crystal centerless ground to 1.975 ± 0.005-inch dia. with <110> flats; (c) <111> GaAs crystal grown with 2 ± 0.060-inch dia. using "coracle" method.

systematic errors in the differential weight gain signal due to significant capillary forces,[6] this growth method results in crystals with diameters which vary (usually within ± 5 mm) along the boule length, as illustrated in Fig. 1a and the trace of the DWS in Fig. 3a. The growth of <100>-oriented crystals with manually controlled diameters has been extended to crystals pulled from larger volume melts. Fig. 2 shows a <100> GaAs crystal grown from a 6-Kg GaAs melt which was synthesized in-situ in a PBN crucible in the Melbourn puller immediately prior to crystal growth. Approximately 96% of the melt was pulled, yielding a <100>-crystal having a mean diameter of 90 mm and a length of 23 cm.

In contrast to the variability associated with manual diameter control, the method of pulling the crystal through a diameter-defining "coracle" offers improved diameter control as indicated by the differential weight signal of Fig. 3b. A limited number of experimental growths have been carried out using the coracle method. The coracle technique is well developed for <111> growths and indicates that diameter uniformities of ± 1.5 mm are achievable as shown by the crystal in Fig. 1c. Device fabrication employing ion implantation or epitaxial techniques is normally carried out on (100) GaAs surfaces. Thus, the <111> coracle technology offers little advantage at the present time since the <111>-oriented crystals would have to be sliced at 54^{o} angles and would thus yield elliptical (100) wafers. In addition, our preliminary assessments of the structural quality of <111>-oriented LEC crystals grown by the "coracle" method (as determined by X-ray topography and dislocation etching techniques) indicate that such crystals are often characterized by excessive dislocation generation and formation of micro-twins near the crystal periphery while extensive activation of <111> [110] glide systems occurs in the interior of the crystal.

Attempts in the past to use the coracle method for <100>-growths have been frustrated by the tendency for <100>-oriented crystals to twin early in the growth.[7] We report here successful <100> coracle growth for the first time as far as we know. Fig. 4 shows a 50-mm diameter

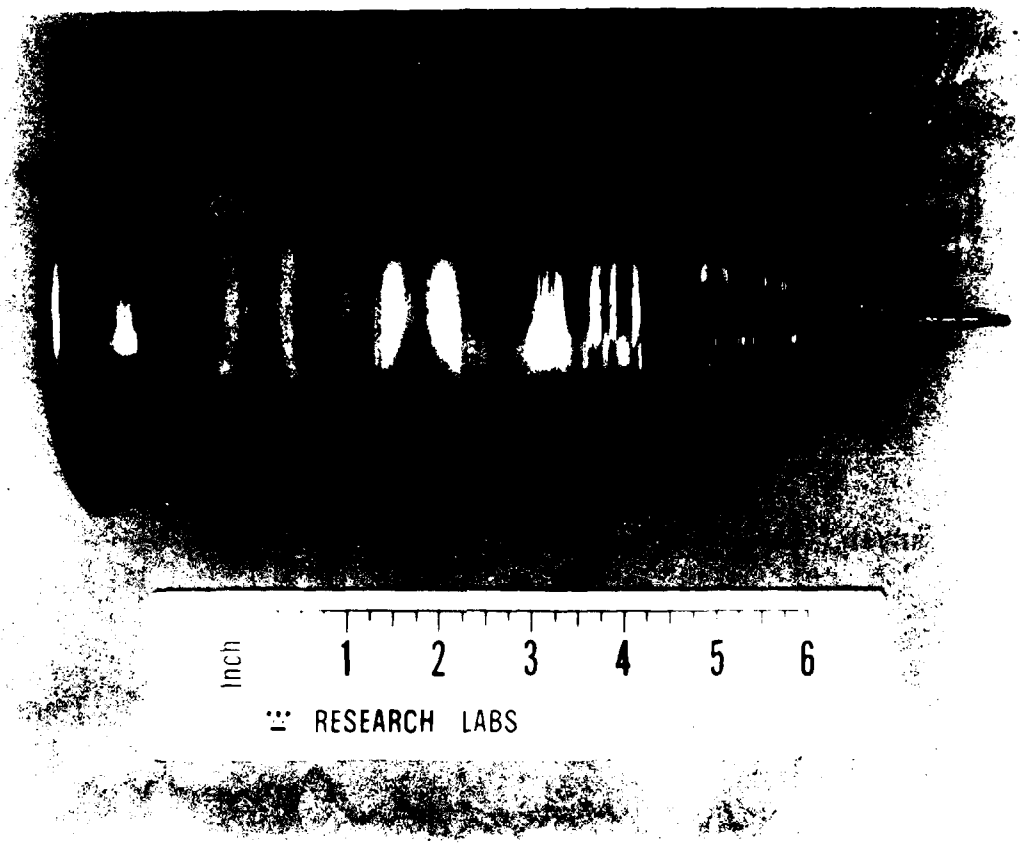

Figure 2 Undoped, semi-insulating <100> GaAs/PBN crystal pulled from 6 kg charge. Mean dia. 90 mm.

Curve 728665-A

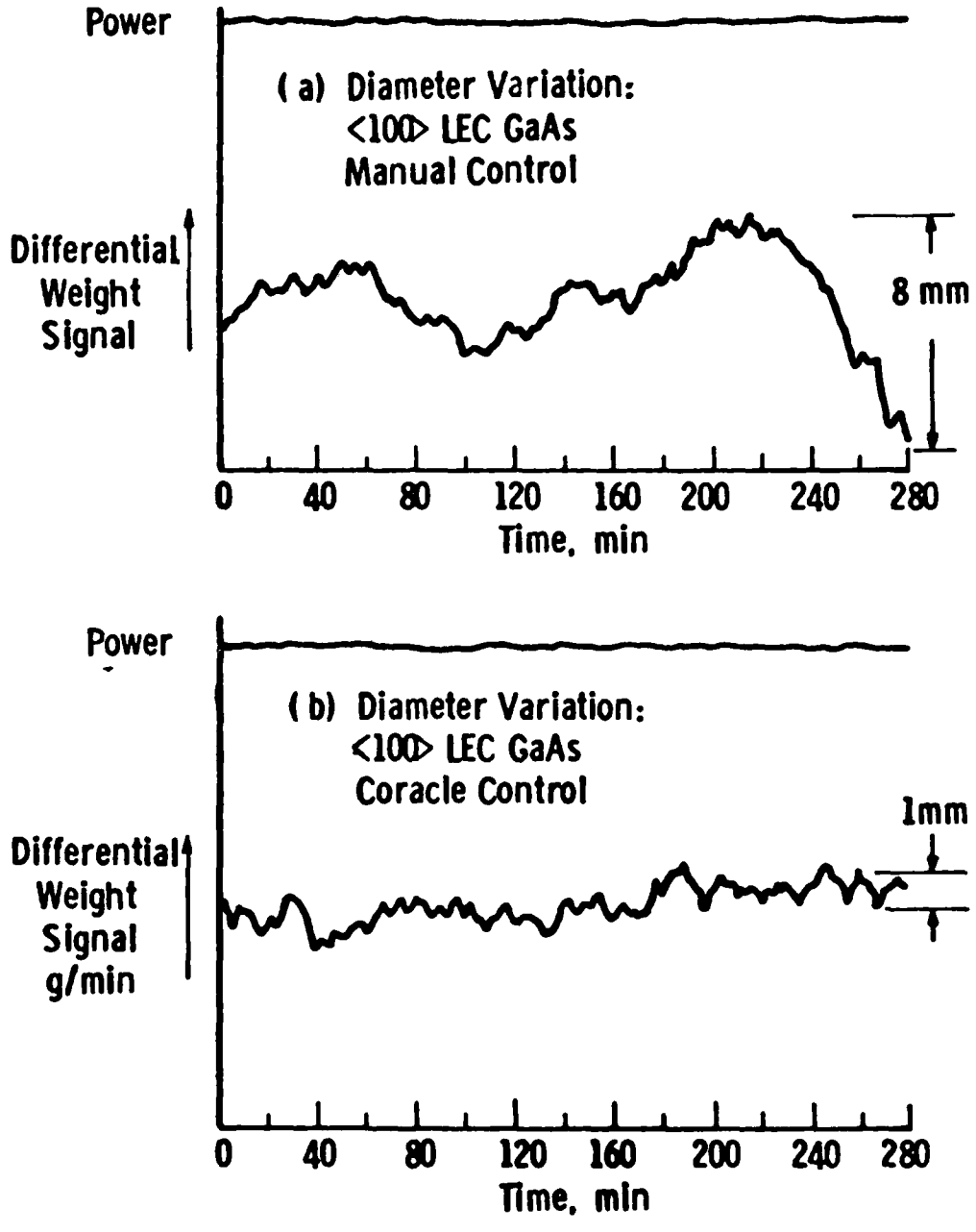

Figure 3 Differential weight gain signals for "manual" diameter control vs. "coracle" dia. control.

'Coracle'-Grown, <100> LEC GaAs

Figure 4 <100>, 50-mm dia., GaAs/PBN crystal grown using "coracle" dia. control.

<100> GaAs crystal grown by the coracle technique. Twinning which normally occurs early in the growth has been delayed to a point approximately halfway along the crystal. (This crystal yielded approximately 60 twin-free substrates with uniform 50-mm diameters.) No evaluation on crystalline quality or impurity content of the substrates is available as yet; however, the results of this experimental growth are encouraging and investigations are continuing.

An alternative approach to achieving uniform, circular cross-section, (100)-oriented GaAs wafers is illustrated in Fig. 1(b) where a <100> ingot has been ground accurately to a 50-mm diameter with a (110) orientation flat by conventional grinding techniques. Surface work damage is removed by etching. Approximately 100 polished wafers of uniform diameter with a thickness of about 0.020 inches can be obtained from a typical 3-Kg, <100>, 2-inch diameter crystal.

2.2 Crystalline Quality

Investigations to improve the structural quality of large-diameter <100> GaAs crystals have concentrated on determining the optimum conditions for initiating a dislocation-free growth and eliminating the tendency toward twinning, which has often frustrated <100> GaAs growth efforts in the past. The growth of GaAs crystals free of twins and having reduced dislocation densities depends upon growth conditions which yield proper stoichiometry,[8] interface shape,[9,10] crystal cone angle,[11,12] and reduced thermal stresses.[13]

2.2.1 Twinning in <100> LEC Growths

It should be noted that twinning especially may result from mechanisms such as local nonstoichiometry, excessive thermal stresses due to variations in crystal diameter, or instabilities in the shape of the crystal growth front associated with the emergence of the crystal through the boric oxide layer. In this regard, the gradual increase of the crystal diameter to the desired value (so that the angle between the

axis and the crystal surface <45°) helps to avoid twinning in the early stages of growth.

To achieve reproducible growths of high-quality, twin-free crystals, a growth procedure was adopted which included the use of vacuum baking of the boric oxide encapsulant to remove residual moisture -- an important factor in maintaining high visability of the melt-crystal interface during growth.[3] There is substantial evidence indicating that the water content of the B_2O_3 encapsulant influences the defect density of LEC crystals. A high frequency of twinning (particularly for <100>-oriented crystals) associated with the use of unbaked, high H_2O-content B_2O_3 in the growth of LEC GaAs crystals has been reported by several workers.[2,3] More recently, Cockayne et al. have definitely related the water content of the B_2O_3 encapsulant to the generation of defect clusters in LEC InP.[15]

Statistics relative to the incidence of twinning for growth with dry (<500 ppm wt OH) and wet (> 1000 ppm wt OH) B_2O_3 are given in Fig. 5 for growths from fused-SiO_2 and PBN crucibles. A crystal is defined as having twinned if it exhibits a twin in the first 75% of growth. For both types of crucibles the incidence of twinning is substantially lower for growths using vacuum-baked B_2O_3 ([OH] <500 ppm).

2.2.2 Dislocation Studies and Thermal Geometry

It has been shown on an experimental basis that crucible-pulled GaAs crystals can be grown free of dislocations at small crystal diameters, usually $\leq$0.5 inches and crystal lengths $\leq$3 inches.[16] For these small crystals, successful dislocation-free growth depends upon the following growth conditions: (1) a Dash-type seeding method in which the seed is grown with a thin neck before increasing the diameter to form the crystal cone[17]; (2) a melt which is close to stoichiometry and a small axial temperature gradient at the interface[8]; and (3) the growth interface maintained flat to convex toward the melt.[18] In addition, the angle of the crystal cone is also important for dislocation-free growth. If the cone angle is too large, dislocation

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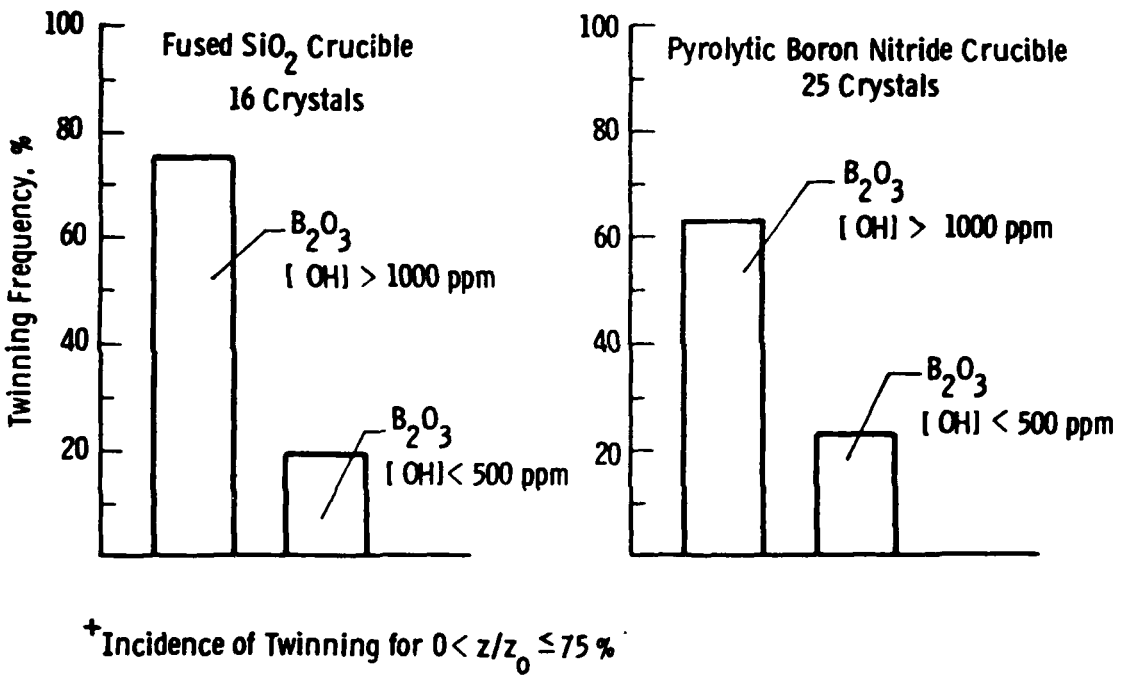


Figure 5 Twinning frequency for <100> GaAs crystals pulled from fused SiO_2 and PBN crucibles.

generation can result from the high internal stresses which develop as the crystal cone emerges from the B_2O_3 encapsulant.[11]

Although GaAs crystals with large cross sections ($\gtrsim$ 50 mm), can be grown free of gross structural imperfections such as twins and inclusions by either Bridgman/Gradient-Freeze or LEC methods, these crystals are usually characterized by high background densities of dislocations (10^4 to 10^5 cm^{-2}) as shown by the reflection X-ray topographs of Fig. 6 for typical large dimension (100) Bridgman and LEC wafers. It can be seen that the density and distribution of dislocations are similar for both Bridgman and LEC growth techniques.

Our preliminary investigations on improving the defect density of large-diameter LEC GaAs crystals have focussed on finding the optimum conditions for initiating dislocation-free growth. Figs. 7(a) and 7(b) show X-ray reflection topographs of longitudinal sections of seed-end cones for two <100> GaAs crystals corresponding to two different cone angles: (a) a relatively shallow cone and (b) a steeper cone of 27° to the crystal axis. In both cases dislocation-free growth is initiated using a Dash-type seeding. As the cone diameter increases, the regions of highest dislocation density ($<10^3$ cm^{-2}) are confined to the crystal interior and a layer near the crystal surface corresponding to regions of maximum thermal stress; however, severe glide plane activation such as that typically observed in flat-top growths[5] has been eliminated. In addition, a steep cone angle like that shown in Fig 7b has been found to reduce dramatically the tendency toward twinning which normally accompanies shouldering in flat-top growths of <100> GaAs crystals.

Large-diameter (< 3-inch) <100> LEC GaAs crystals are characterized by radially nonuniform dislocation distributions exhibiting maximum dislocation densities in the 10^4 to 10^5 cm^{-2} range at the center and periphery of the crystal with a minimum at ~0.6r as shown in Fig. 8. The dislocation-generation mechanism in large diameter crystals (>2 cm) is thought to be due primarily to thermally induced stresses which

SEMI-INSULATING GaAs HORIZONTAL-BRIDGMAN

(a) X-ray reflection topograph, g= (315). Area = 0.41 cm^2

SEMI-INSULATING GaAs LEC/PBN

(b) X-ray reflection topograph, g = (315). Area = 0.41 cm^2

Figure 6 Comparison of dislocation distribution in Bridgman-grown and LEC substrates of approximately equal areas.

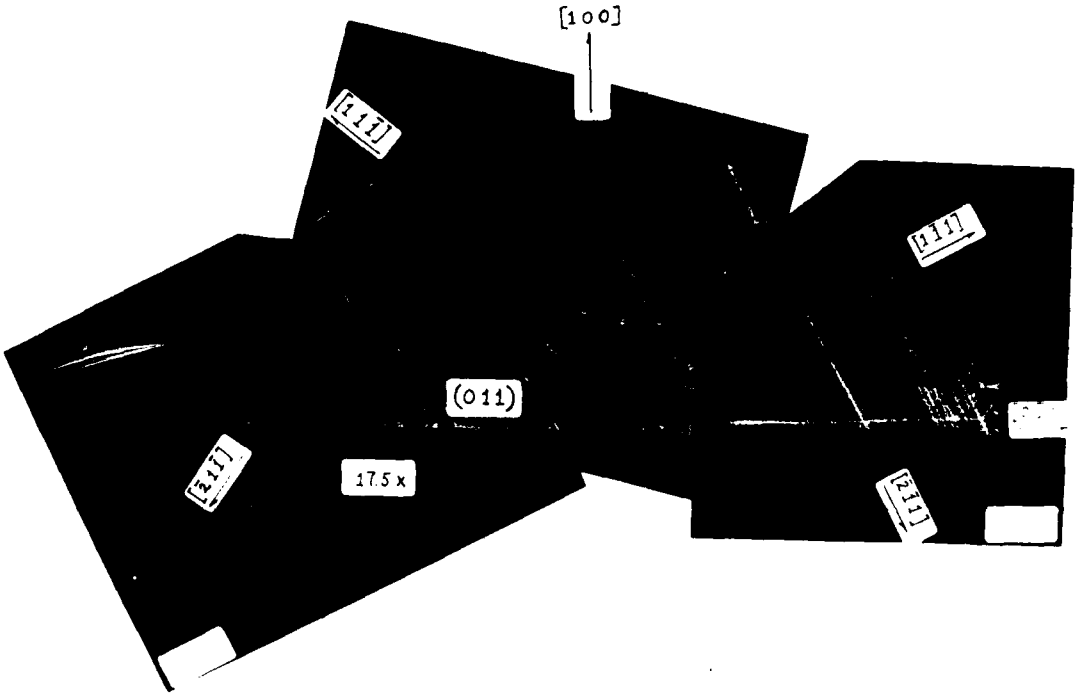


Figure 7a Reflection X-ray topograph (g = <315>) of (011) longitudinal section for a shallow cone angle. Crystal pulled from pyrolytic boron nitride crucible.

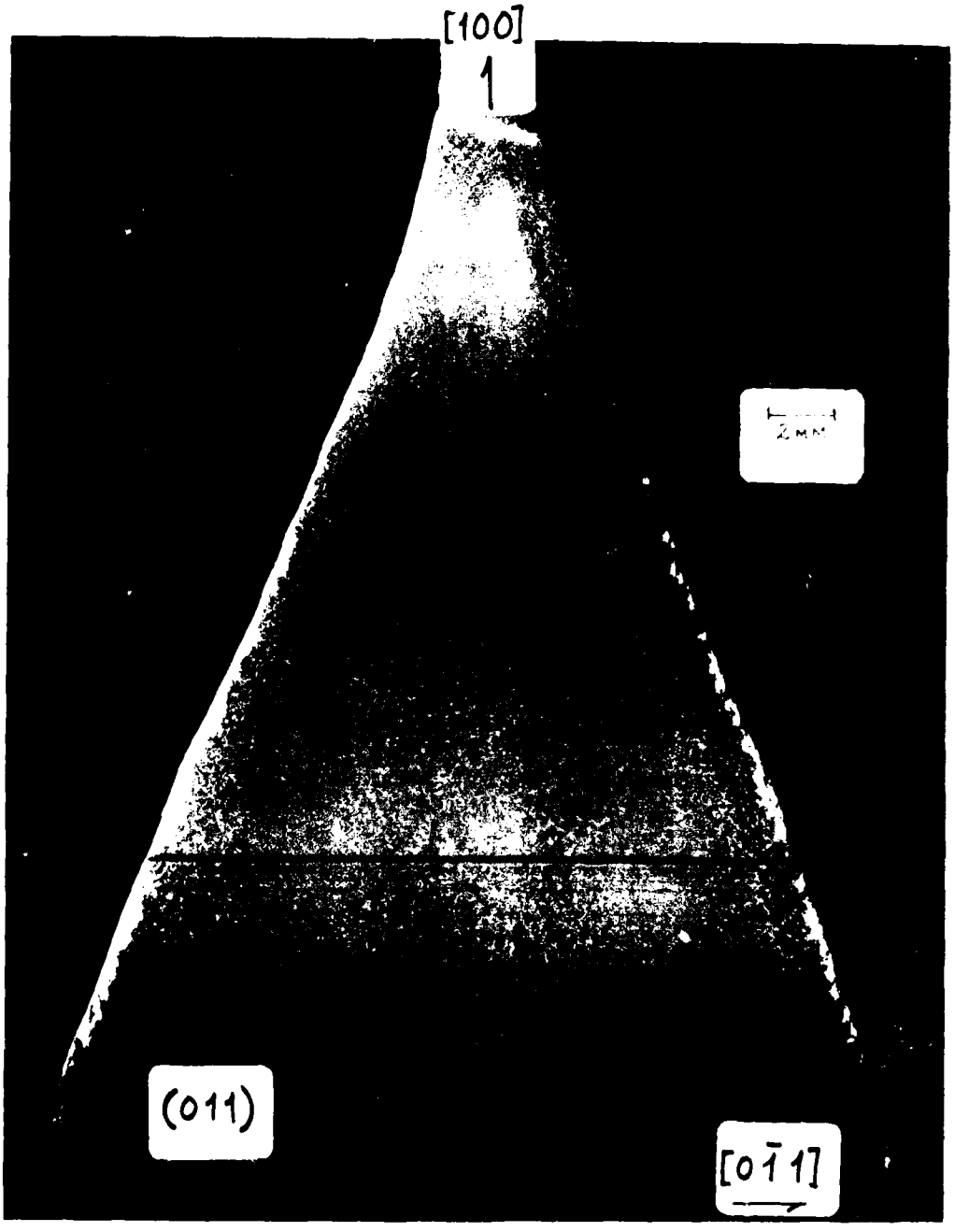


Figure 7b Reflection X-ray topograph (g = <260>) of (011) longitudinal section for cone angle of 27°. Crystal pulled from pyrolytic boron nitride crucible.

Curve 728662-A

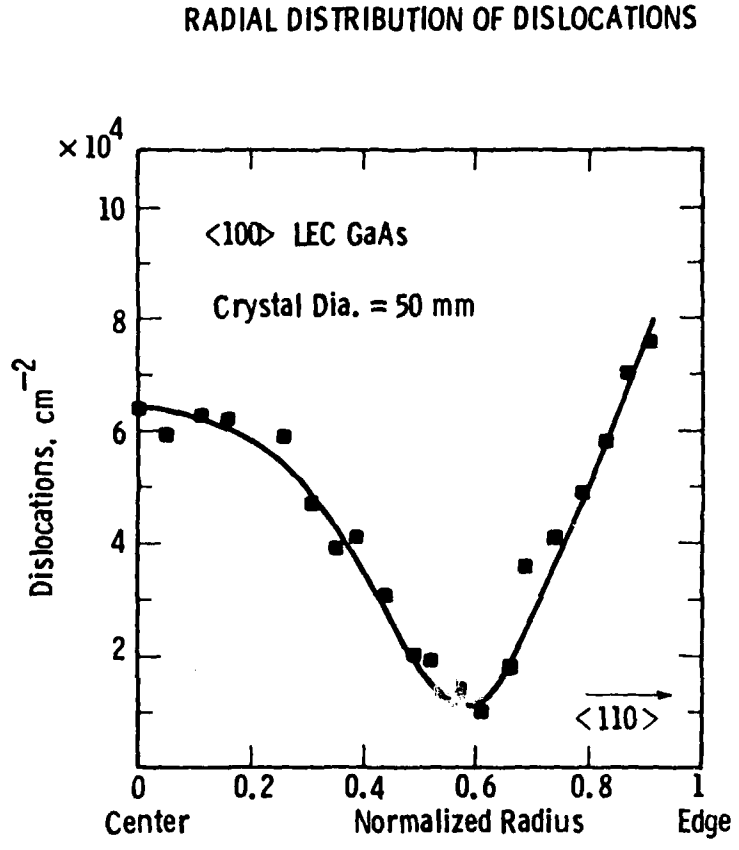


Figure 8 Radial distribution of dislocations in typical 50-mm dia. LEC <100> GaAs/PBN crystal.

accompany large axial and radial temperature gradients, owing to the large convective heat transfer coefficient of the B_2O_3 encapsulating layer and the temperature difference between the crystal interior and the B_2O_3 ambient near the growth interface.[13] In contrast to Czochralski-grown silicon crystals, which can withstand a factor of three higher stress[19] and still be grown dislocation-free even at diameters up to 100 mm, the resulting thermal stresses associated with the LEC growth of GaAs can easily exceed the critical resolved shear stress for dislocation motion near the melting point. Dislocation-free growth is achieved easily only for GaAs crystals with diameters $\lesssim$ 15 mm, where the attendant thermal stresses are significantly diminished.[13]

In the LEC growth system the magnitudes of the axial and radial temperature gradients existing at the melt/B_2O_3 interface and across the boric oxide layer itself are known to play a dominant role in determining whether or not the crystal will dislocate at the growth interface or during the time required for the crystal to transit the boric oxide layer thickness.[9,13] Reducing these gradients should lead to a corresponding reduction in the defect density. A question to be answered then is which growth parameters available to the operator offer the best possibility of reducing the temperature gradients at the growth interface? Among the parameters which are easily variable are: (1) the starting crucible position with respect to the heat zone, (2) the pressure of inert ambient growth, and (3) the species of the inert ambient and thus its thermal conductivity. Changes in either of these parameters or in combination would be expected to produce changes in the axial and radial gradients of the system.

Thermal profiles along the geometric axis of the Melbourn crystal puller in the absence of actual crystal growth are shown in Figs. 9(a) and 9(b) for various operating conditions. The profiles were measured with reference to the crucible bottom and extend through the GaAs melt, the B_2O_3 encapsulating layer (~20 mm thick), and 5 cm into the inert argon ambient above the encapsulant. Even though the

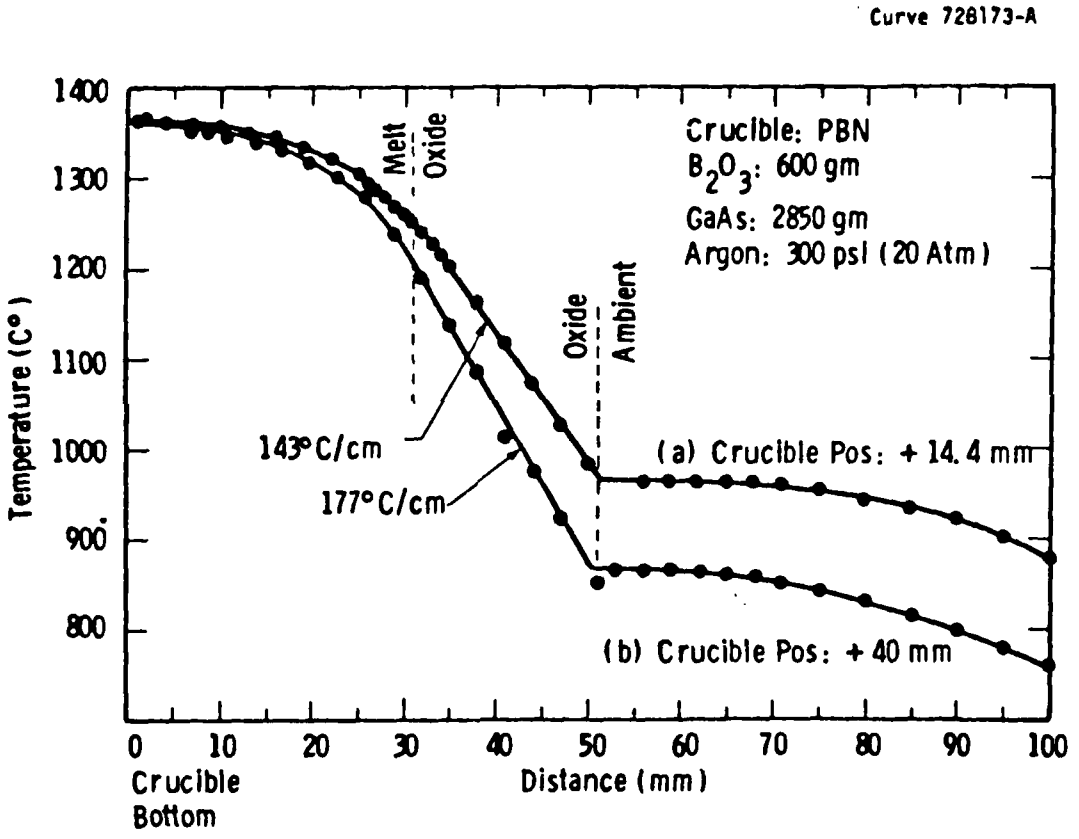


Figure 9a Thermal profiles along the geometric axis of the Melbourn LEC system in absence of crystal growth. Ambient pressure: 300 psi.

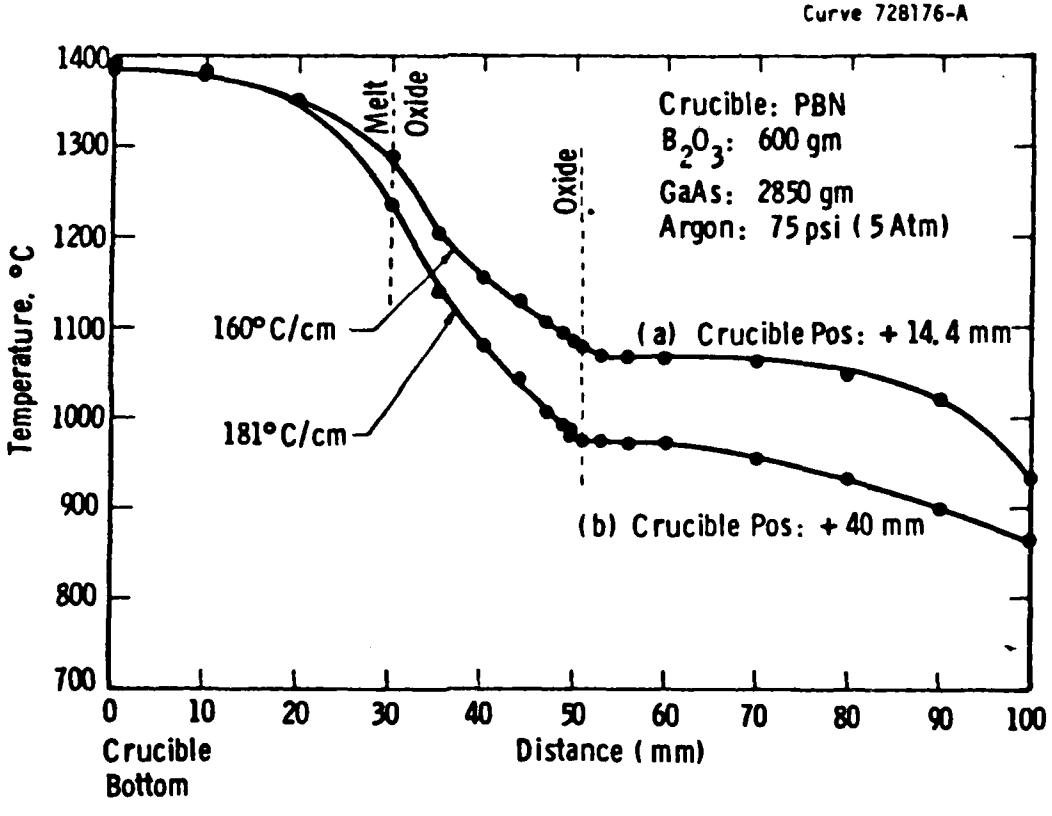


Figure 9b Thermal profiles along the geometric axis of the Melbourn LEC system in absence of crystal growth. Ambient pressure: 75 psi.

measurements were made in the absence of actual crystal growth (where effects due to latent heat dissipation and conduction that heat up the growing crystal can significantly modify the thermal gradient at the growth interface), a knowledge of the relative change in temperature across the system of melt/B_2O_3/ambient under conditions of predominantly radiative heat losses is instructive. Such conditions should approximate those corresponding to the early stages of LEC growth when the crystal is totally submerged in the B_2O_3 encapsulant. An axial thermal gradient of ~140°C/cm (upper curve of Fig. 9a) was measured across the B_2O_3 layer for normal operating conditions (i.e., PBN crucible low in heat zone, ambient pressure 20 atm.) When the crucible is moved up ~25 cm in the heat zone, the gradient increases to ~180°C/cm owing to the 200°C greater cooling at the surface of the B_2O_3. The sensitivity of the B_2O_3 surface to changes in ambient pressure is reflected in the thermal profiles of Fig. 9b, which correspond to a factor of four-fold reduction in pressure. For both crucible positions, the surface temperature of the B_2O_3 increases by ~100°C when the ambient pressure is dropped from 20 atm to 5 atm. However, the thermal gradient near the GaAs melt surface is relatively unaffected. Moreover, growths carried out under 5-atm pressure yield crystal surfaces with severe decomposition owing to the higher ambient temperature. The insensitivity of the gradient across the B_2O_3 layer to variations in crucible position and ambient pressure is surprising and indicates that varying the B_2O_3 thickness itself offers the best possibility of reducing the axial temperature gradient at the melt/B_2O_3 interface. This observation is supported by a similar recent finding of Shinoyama et al.[20] on the growth of dislocation-free LEC crystals of InP.

2.2.3 Microuniformity of LEC GaAs Crystals

The effects on device performance caused by microscopic nonuniformities such as impurity striations and microprecipitates are of concern for processing over large-area substrates in microwave small signal, power, and logic-circuit applications. Preliminary investigations

on impurity-striation behavior in large-diameter LEC GaAs crystals have been carried out. For this study, (111) cross sections sliced from 50-mm diameter <100>-oriented LEC GaAs crystals were polished to a mirror finish in Br-methanol and then etched in an A-B solution to reveal longitudinal striations. The samples were examined under a Nomarski constrast interferometer. Fig. 10 shows longitudinal striations (presumably due to microvariations in resistivity) for: (a) undoped semi-insulating GaAs grown from PBN crucibles and (b) low-resistivity n-type crystals pulled from fused-SiO_2 crucibles. In the case of the semi-insulating GaAs/PBN crystal (Fig. 10a), the impurity content is extremely low, implying that the observed striations may arise from local fluctuations in stoichiometry.[11] The closely spaced striations in the low-resistivity, n-type material (Fig. 10b) result from variations in dopant incorporation (in this case Si, $K_o \sim 0.1$, introduced from the SiO_2 crucible) due to fluctuations in microscopic growth rate. An even greater axially striated impurity distribution and greater microscopic nonuniformity would be expected for Cr-doped GaAs since chromium has a very low segregation coefficient, $K_o \sim 6 \times 10^{-4}$.

Fluctuations in the microscopic growth rate in Czochralski crystal growth arise because of thermal asymmetries at the crystal-growth interface. Symmetrical or rotational impurity striations are almost always observed for impurities with effective segregation coefficients differing significantly from unity because of the seed/crucible rotation which is conventionally employed. Nonrotational striations which are caused mainly by turbulent thermal-convection flows in the melt become increasingly important in large-volume melts.[21] The convective flows corresponding to a system consisting of a large-volume GaAs melt (viscosity 0.1 poise) surrounded by a relatively viscous (30 poise) B_2O_3 encapsulant situated in a high-pressure (20 Atm) gas ambient are probably characterized by large Rayleigh numbers. Temperature fluctuations due to convective turbulence in the melt would be quite severe.

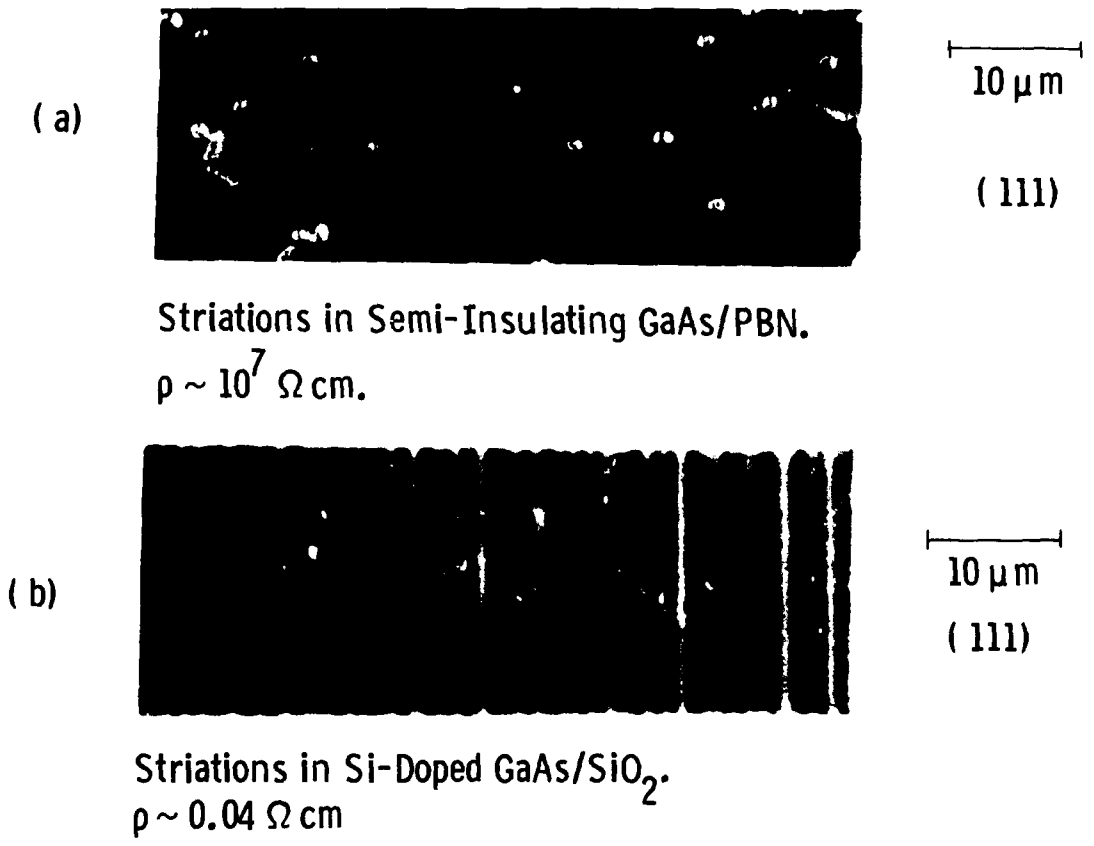


Figure 10 Longitudinal striations in (100) LEC GaAs crystals.

Temperature fluctuations observed in a 6-inch diameter, 3-kg, B_2O_3-encapsulated GaAs melt in the high-pressure Melbourn system are shown in Fig. 11. To our knowledge, this is the first time that thermal fluctuations in large-volume LEC GaAs melts have been investigated. The melt was contained in a PBN crucible which was rotated at 15 rpm. The inert argon ambient was held constant at 20 Atm. The measurements correspond to positions along the geometric axis of the system. Temperature fluctuations at the B_2O_3/GaAs interface (Fig. 11a) display a ΔT_{max} > 3°C with individual temperature excursions > 2°C. Over the total 8-min time interval monitored, a systematic variation is observed with a large period of ~1 min. Superimposed on this course periodicity is a more rapid fluctuation with a frequency of approximately 10 temperature excursions per min. Fig. 11b shows the thermal fluctuations observed under the same conditions for a position of ~1/cm below the surface of the GaAs melt. Here the amplitude of the fluctuations is much larger than at the B_2O_3/GaAs interface. ΔT_{max} is 9°C with individual excursions as large as 6°C. The fluctuation frequency is also higher than at the interface, ~20 excursions per min. The large magnitude of the temperature variations implies a much higher degree of convective turbulence for the encapsulated GaAs melt relative to large-volume silicon melts. In this regard, as has already been demonstrated for silicon melts[22,23] the application of magnetic fields across large-volume LEC GaAs melts could have important beneficial effects on the suppression of thermal fluctuations and corresponding improvements in microuniformity.

Undoped and Cr-doped (100) LEC GaAs substrates grown in the Melbourn LEC system have also been analyzed for indications of microprecipitation. Fig. 12(a) shows a (100) substrate surface of an undoped LEC GaAs/PBN wafer which was etched using an A-B etchant.[24] No microprecipitates are revealed in the dislocation-free areas of the substrate matrix; however, small features with diameters of ~1 to 2 microns could be observed decorating the dislocation lines themselves as shown in Fig. 12b. These features are speculated to be As precipitates,

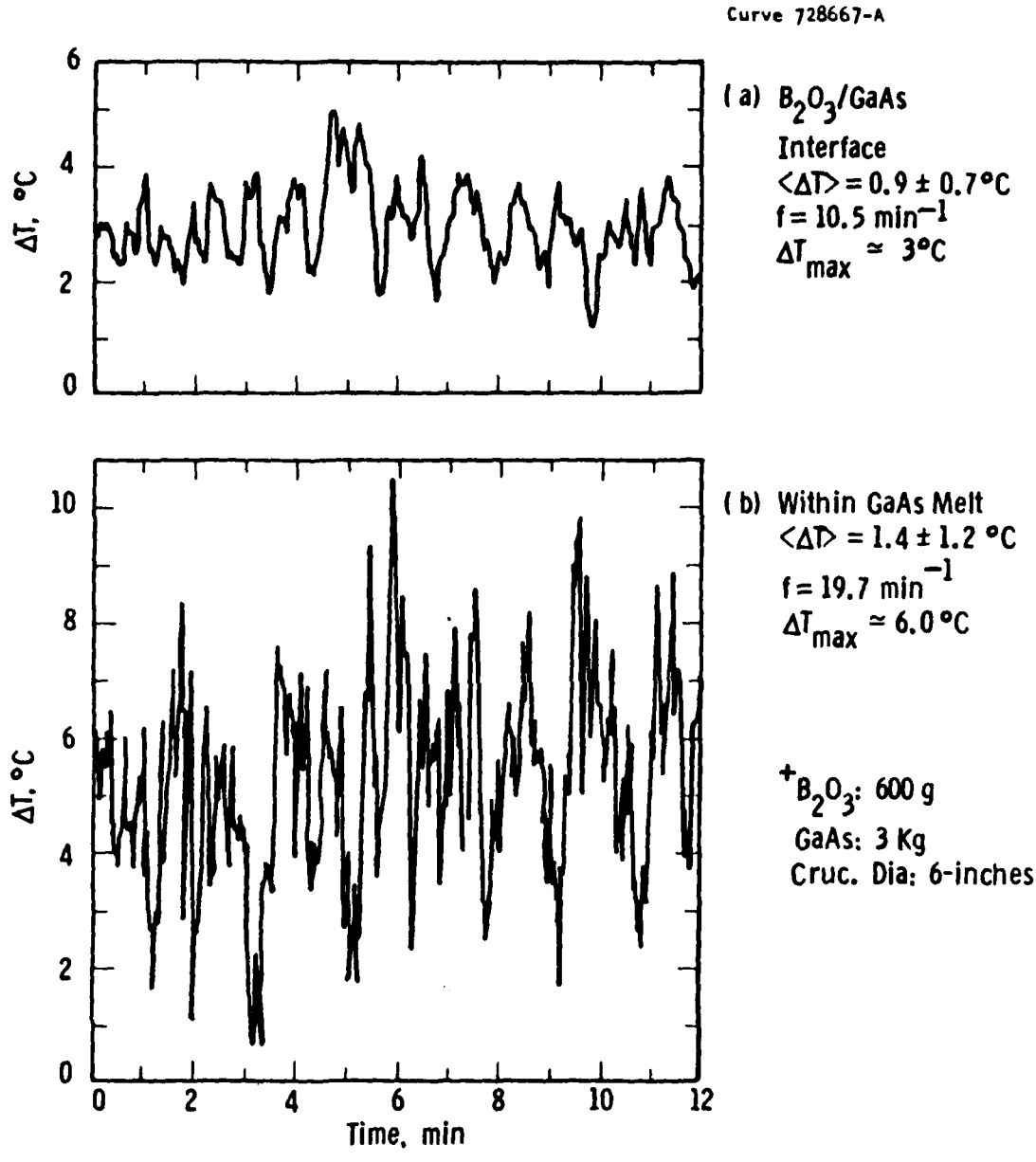
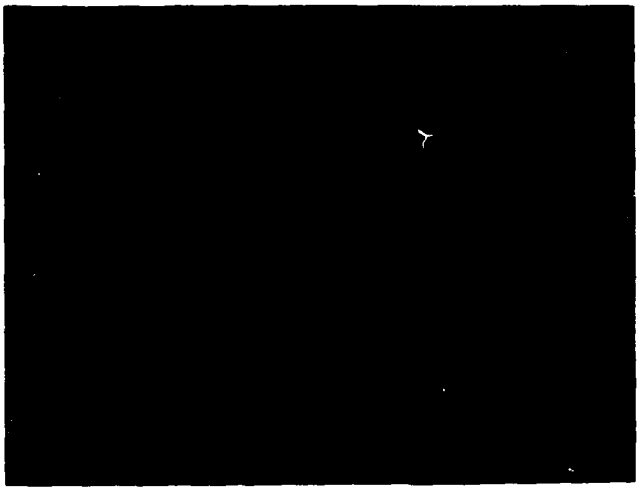


Figure 11 Temperature fluctuations in large-diameter liquid-encapsulated GaAs melt.



(a) Dislocations lying in (100) surface of LEC GaAs/ PBN wafer. A-B etchant.

(b) Dislocation line showing decoration due to As precipitates.

Figure 12 (a) Dislocations lying in (100) surface of LEC GaAs/PBN wafer. A-B etchant. (b) Dislocation line showing decoration due to As precipitates.

based on a similar observation by Cullis et al.,[25] who postulate that the segregation of As precipitates along the dislocation lines takes place by condensation of As point defects (interstitials) from the surrounding lattice. This observation suggests that a high point defect concentration can exist in LEC crystals (10^{16} to 10^{17} cm^3), and that As exists as an important mobile point defect species in GaAs. This latter inference has important implications in regard to the effect of thermal annealing on deep levels in GaAs (see Section 4.4).

Gallium inclusions can sometimes be observed near the periphery of LEC GaAs crystals whenever the crystals exhibit diverging surfaces. In Fig. 13 a ring of bright points (gallium inclusions) can be seen ~1 mm inside the periphery of a <100> GaAs substrate sliced from the conical seed end of a crystal. The pronounced rectangular shape of the wafer is an artifact of the growth habit near the seed end of the crystal. The origin of the Ga inclusions is thought to be due to thermomigration of liquid Ga droplets along the <100> growth direction and is a variation of the temperature-gradient zone melting (TGZM) mechanism.[26] The mechanism for the migration is speculated to be as follows: owing to some dissociation of the crystal surface during growth, liquid gallium nuclei can form on those portions of the crystal surface which diverge from straight-sided growth. In contact with the solid GaAs in the presence of the temperature gradient dT/dZ across the B_2O_3 encapsulating layer, the liquid Ga will dissolve some GaAs owing to the solubility of GaAs in liquid Ga at a given temperature.[27] The solubility of GaAs is greater at the front surface of the inclusion where the temperature is higher than at the rear of the inclusion. A concentration gradient of As is set up across the volume of the inclusion. Arsenic diffuses toward the cooler interface at the rear of the inclusion, and a layer of GaAs freezes out at the rear. Continuation of the solution-diffusion-freezing action causes the liquid Ga inclusion to migrate through the GaAs in the <100> growth direction, i.e., the direction of the axial temperature gradient. The main factors influencing the rate of travel of the liquid Ga inclusion are: (1) the

(a) (100) 2-inch dia. LEC GaAs wafer showing peripheral gallium inclusions

(b) (011) longitudinal cross-section of LEC GaAs crystal cone near periphery showing gallium inclusions

Figure 13 (a) (100) 2-inch dia. LEC GaAs wafer showing peripheral gallium inclusions. (b) (011) longitudinal cross section of LEC GaAs crystal cone near periphery showing gallium inclusions.

magnitude of the temperature gradient dT/dZ across the B_2O_3 layer, (2) the diffusivity of As in liquid Ga, and (3) the slope of the liquidus $\frac{dT}{dX_{As}}$. A high travel rate is favored by large dT/dZ and D, and small dT/dX_{As}.[26] As shown in Fig. 13b, migration tracks up to 200 microns long have been observed at the periphery of some LEC GaAs crystals.

2.3 GaAs Substrate Preparation

Substrate preparation is a critical step in the direct ion-implantation technology for GaAs. The substrate preparation methodology used in our work is outlined in this section.

The <100>-oriented GaAs crystals are accurately centerless-ground to 50-mm diameter and provided with two <110>-orientation flats (as shown in Fig. 1b) to distinguish front and back wafer surfaces. The ground and flatted ingots are then mounted in an ultra-low vibration saw (8-inch ID) for automatic wafering. This machine is equipped with a universal table and goniometric settings which allow precise alignment of the ingot for the desired substrate orientation. The exact orientation of a test slice is verified by X-ray diffraction, and the entire ingot is then wafered using conventional automatic slicing procedures. Typical as-sliced wafer thickness is 670 ± 10 microns.

The presence of liquid gallium inclusions near the periphery of as-grown substrates sliced from unground LEC GaAs crystals exhibiting diverging surfaces can be troublesome for whole-wafer device processing and high-temperature fabrication steps owing to gallium contamination of the polished wafer surface. In this regard, an additional advantage of the centerless-grinding operation is that any peripheral gallium inclusions associated with diverging surface areas of the crystal are entirely removed during the grinding operation.

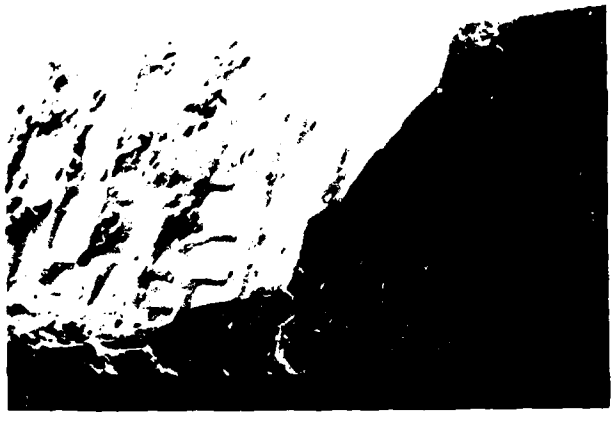
In preparation for device processing, the wafers are lapped by conventional lapping methods and then polished on front and back surfaces using a diluted bromine (0.2%) methanol technique on a smooth-napped polishing pad to a final wafer thickness of 500 microns. For

this technique, wafer thickness variations of ± 10 microns across a 50-mm diameter wafer are typical.

Immediately after polishing and rinsing in hot semiconductor (low-mobile ion)-grade trichlorethane, acetone, and propanol, the wafers are spin-scrubbed using a standard commercial silicon wafer scrubber in order to remove particulates which can easily adhere to the semi-insulating substrates. In order to minimize exposure of the polished wafer surface to particulates and atmospheric contamination, the wafers are immediately capped with Si_3N_4 prior to the implantation process. The capping technique is described in Section 5.

In addition to the wafer preparation steps outlined above, edge-rounding of GaAs wafers (a processing step routinely utilized in the silicon industry for reducing wafer chipping and breakage during cassette-to-cassette handling) has been investigated and successfully demonstrated at the Westinghouse R&D Center for 50-mm and 75-mm diameter GaAs wafers sliced from centerless ground boules. Fig. 14a is an SEM micrograph showing the peripheral edge of a cleaved, unground, as-grown LEC GaAs substrate exhibiting microcorrugation and pitting characteristic of the as-grown LEC boule surfaces. It is speculated that these irregularities in the wafer edge can act as regions of high stress and sources of microcracks which assist in easy wafer fracturing under edge impact. It is well established that edge-rounded silicon wafers can withstand up to three times the edge impact force normally sustained by as-grown wafers.[28] Fig. 14b shows the peripheral edge of a cleaved LEC GaAs wafer sliced from a centerless-ground boule and edge-rounded for uniform edge curvature. Studies are currently underway to quantitatively assess the effectiveness of edge-rounding of GaAs wafers in reducing breakage and edge chipping.

a. Without Edge-rounding



b. Edge-rounded

Fig. 4 — SEM photographs of polished GaAs wafers

Figure 14 SEM micrographs of peripheral edge of: (a) as-grown LEC GaAs substrate; (b) centerless ground and edge-rounded LEC GaAs substrate. Wafer thickness: 20 mil.

3. CRYSTAL PURITY

3.1 Impurity Content By SIMS Analysis

Secondary ion mass spectrometry (SIMS) bulk analysis of LEC GaAs material pulled from both quartz and pyrolytic boron nitride (PBN) crucibles at our laboratories, as well as commercially supplied large-area boat-grown substrates and LEC GaAS pulled from quartz containers has been carried out. A wide range of impurity species were examined. The SIMS data (Tables I and II) taken together with the resistivity data on corresponding substrates show clearly that LEC growths from PBN crucibles yield reproducibly high-purity GaAs substrates exhibiting consistently high, thermally stable semi-insulating behavior. Undoped GaAs crystals pulled from quartz crucibles often exhibit variable and anomalously low as-grown resistivities, while commercially supplied Cr-doped, semi-insulating GaAs substrates are characterized by impurity contents which vary from supplier to supplier. The detailed SIMS data for crystals pulled from pyrolytic boron nitride crucibles is shown in Table I. Quantitative estimates of impurity concentrations were obtained by calibration against GaAs samples which had been implanted with known doses of specific impurities. Comparative SIMS results for LEC GaAs pulled from PBN and quartz crucibles and boat-grown substrate material are shown in Table II. For LEC GaAs prepared at our laboratories, residual silicon concentrations in the mid-10^{14} cm^{-3} range are observed in GaAs/PBN samples and somewhat higher concentrations in crystals pulled from quartz crucibles. Commerically supplied LEC and boat-grown crystals grown in quartz containers exhibit silicon levels which range up to mid 10^{16} cm^{-3}, depending upon growth technique and the substrate supplier. The residual chromium content in undoped LEC GaAs crystals pulled from either PBN or fused-silica crucibles is below the detection limit of the SIMS instrument, estimated to be in the low

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TABLE I –HIGH SENSITIVITY SECONDARY ION MASS SPECTROSCOPY ANALYSIS †
OF LEC SEMI-INSULATING GaAs CRYSTALS PULLED FROM HIGH PURITY
PYROLYTIC BORON NITRIDE CRUCIBLES

Crystal	C*	O*	Si	S	Se	Te	Cr	Mg	Mn	B	Doped Yes	Doped No
BN-1 (s)	2 e 15	1.5 e 16	4.8 e 14	5.7 e 14	2 e 13	1 e 12	< 4 e 14	1 e 15	7 e 14	2.3 e 15		✓
BN-2 (s)	1 e 16	6 e 16	6 e 14	2 e 15	1 e 15	7 e 13	5.6 e 14	4 e 14	8 e 14	1.7 e 17		✓
BN-3 (s)	3 e 15	1.3 e 16	9.3 e 14	4.2 e 14	3 e 14	<5 e 12	4.3 e 14	2 e 15	1 e 15	5.4 e 17		✓
BN-4 (s)	-	-	2 e 15	8 e 14	2 e 14	1 e 14	1 e 16	2.5 e 15	2 e 15	1.5 e 17	Cr	
BN-6 (t)	2.9 e 15	9.8 e 15	5.4 e 14	5 e 14	9.4 e 13	<5 e 12	5.4 e 14	2.5 e 15	1.7 e 15	6.9 e 17		✓
BN-10 (s)	2 e 15	1 e 16	8.6 e 14	1.5 e 15	7 e 14	7 e 12	< 4 e 14	3.6 e 15	1.2 e 15	2 e 18		✓
BN-11 A (s)	4.3 e 15	1.8 e 16	6.4 e 14	1 e 15	8 e 13	6 e 12	6.4 e 15	3.2 e 15	1.4 e 15	1.9 e 17	Cr	
BN-11 B (s)	3 e 15	1.3 e 16	7.6 e 14	8.7 e 14	1 e 14	8 e 12	6.3 e 15	4.4 e 15	1.6 e 15	1.9 e 17	Cr	
BN-12 (s)	2 e 16	7 e 16	1 e 15	2 e 15	5 e 14	6 e 13	3.2 e 15	3 e 14	8 e 14	1.8 e 17	Cr	
BN-13 (s)	-	-	< 3 e 14	4 e 15	2 e 14	1 e 13	2 e 15	5 e 14	7 e 14	7 e 16	Cr	
BN-13 (t)	-	-	< 3 e 14	3 e 15	5 e 14	1 e 13	4 e 15	8 e 14	7 e 14	2 e 17	Cr	
BN-14 (s)	-	-	4 e 14	8 e 14	9 e 14	8 e 12	6 e 14	1 e 15	8 e 14	3 e 17		✓
BN-14 (t)	-	-	7 e 14	1 e 15	1 e 15	1 e 13	1 e 15	9 e 14	1 e 15	7 e 17		✓
BN-15 (s)	-	-	< 3 e 14	1 e 15	1 e 14	9 e 12	3 e 15	7 e 14	8 e 14	7 e 16	Cr	
BN-15 (t)	-	-	< 3 e 14	2 e 15	5 e 14	2 e 13	5 e 15	1 e 15	8 e 14	2 e 17	Cr	
BN-18 (s)	-	-	4 e 14	< 3 e 14	7 e 13	1 e 14	3 e 15	< 3 e 14	< 7 e 14	6 e 16	Cr	
BN-20 (s)	-	-	3 e 14	6 e 14	8 e 13	6 e 13	2 e 15	9 e 13	< 7 e 14	1 e 17	Cr	
BN-21 (s)	-	-	2 e 15	< 3 e 14	3 e 13	7 e 13	3 e 15	-	-	9 e 16	Cr	
BN-22 (s)	-	-	9 e 14	6 e 14	1 e 14	6 e 13	1 e 15	5 e 13	< 7 e 14	2 e 16	Cr	
BN-23 (s)	9 e 15	5 e 16	1 e 15	7 e 14	3 e 14	3 e 13	< 2 e 15	< 3 e 14	1 e 15	1 e 17		✓
BN-28 (s)	1 e 16	6 e 16	1 e 15	1 e 15	3 e 14	3 e 13	4 e 14	< 3 e 14	8 e 14	6 e 16		✓
Detection Limit	-	-	3 e 14	3 e 14	5 e 12	5 e 12	4 e 14	3 e 14	7 e 14	8 e 12		

Sims analysis courtesy Charles Evans & Associates, San Mateo CA
(s) Seed end sample
(t) Tang end sample
* Detection limits for C, O, Fe (<mid 10^{15} cm^{-3}) not well defined

Dwg. 1715807

TABLE II – HIGH SENSITIVITY SECONDARY ION MASS SPECTROSCOPY ANALYSIS† OF GaAs CRYSTALS GROWN BY LEC AND BOAT GROWTH METHODS

Crystal	C	O	Si	S	Se	Te	Cr	Mg	Mn	B	Doped Yes	Doped No
LEC/PBN (a)	5 e 15	2 e 16	5 e 14	1 e 15	4 e 14	1 e 13	4 e 14	7 e 14	8 e 14	5e 17		✓
LEC/QTZ (b)	6 e 15	–	1 e 15	2 e 15	3 e 14	4 e 13	2 e 16	2 e 14	8 e 14	1 e 15	Cr ✓	
	8 e 15	4 e 16	7 e 14	2 e 15	3 e 13	4 e 13	5 e 14	3 e 14	7 e 14	1 e 15		✓
	7 e 15	4 e 16	9 e 14	9 e 14	7 e 13	3 e 13	5 e 14	3 e 14	6 e 14	3 e 15		✓
	5e 16	4 e 16	8 e 14	1 e 15	2 e 14	5 e 13	1 e 16	5 e 14	7 e 14	2 e 15	Cr ✓	
	8 e 16	3 e 16	2 e 15	2 e 15	4 e 13	2 e 13	1 e 16	5 e 14	8 e 14	1 e 15	Cr ✓	
LEC/QTZ (c)	–	–	5 e 15	6 e 15	5 e 14	5 e 13	2 e 16	2 e 15	3 e 15	2 e 15	Cr ✓	
	–	–	8 e 15	4 e 15	4 e 14	4 e 13	6 e 16	3 e 15	2 e 15	2 e 15	Cr ✓	
	–	–	4 e 16	4 e 15	9 e 14	4 e 14	1 e 15	2 e 15	1 e 15	1 e 15		✓
	–	–	2 e 15	5 e 15	3 e 13	7 e 13	3 e 16	2 e 15	1 e 15	1 e 15	Cr ✓	
Boat Grown (c)	–	–	8 e 15	3 e 15	3 e 14	2 e 13	2 e 16	2 e 15	1 e 15	1 e 14	Cr ✓	
	–	–	6 e 15	6 e 15	3 e 14	2 e 13	4 e 16	1 e 15	1 e 15	6 e 14	Cr ✓	
	–	–	2 e 16	8 e 15	2 e 13	4 e 15	9 e 16	2 e 15	2 e 15	7 e 14	Cr ✓	
	–	–	5 e 15	3 e 15	5 e 13	5 e 13	2 e 16	1 e 15	2 e 15	1 e 15	Cr ✓	

(a) Representative of the Values Shown in Table I

(b) Material Prepared In-House

(c) Material from Commercial Suppliers

† Sims Analysis Courtesy Charles Evans & Assoc., San Mateo, CA.

10^{14} cm^{-3} range. Analyses of LEC-grown crystals pulled from Cr-doped melts contained in quartz crucibles reveal that the Cr content (typically 2×10^{16} cm^{-3} at the seed end and approaching 10^{17} cm^{-3} at the tang end) is close to the anticipated doping level based on the amount of Cr dopant added to the melt and its reported segregation behavior.[29] Cr dopant levels of (2 to 9) $\times$ 10^{16} cm^{-3} were observed in material grown by horizontal gradient freeze or Bridgman methods. The reduced concentration of shallow donor impurities in growths from PBN crucibles permits lower Cr-doping levels to be utilized as shown in Table I (BN-11, 12, 13, 15, 18, 20, 21, 22), where typical Cr dopant concentrations range from 3×10^{15} cm^{-3} at the crystal seed end to 6×10^{15} cm^{-3} near the crystal tang end. The SIMS studies also indicate that LEC growths from PBN crucibles generally result in high boron concentrations (10^{17} cm^{-3} range) in the GaAs/PBN material versus low 10^{15} cm^{-3} concentrations in quartz crucible growth. No significant differences in carbon ($\sim 10^{16}$ cm^{-3}), oxygen (10^{16} cm^{-3}), selenium (mid-10^{14} cm^{-3}), tellurium ($<10^{14}$ cm^{-3}), and iron (mid-10^{15} cm^{-3}) contents of different GaAs samples are revealed by these investigations; however, the results for carbon and oxygen must be viewed as tentative since detection limits for these elements are not as yet well defined for the SIMS technique.

The influence of the water content in the B_2O_3 encapsulant on the incorporation of impurities, particularly Si and B, for growths from fused-SiO_2 and PBN crucibles is shown in Fig. 15. For growths from fused-SiO_2 crucibles (Fig. 15a), the Si and B content of the GaAs (as measured by SIMS) is a function of the OH content of the B_2O_3 encapsulant, with B_2O_3 having high-OH content (>1000 ppm OH) yielding lower values of Si and B, while concentrations of B and Si in the mid-10^{16} cm^{-3} range have been observed for growths utilizing vacuum-baked B_2O_3 (<500 ppm OH). The chemical kinetics controlling the apparently linear relationship between Si and B in growths from SiO_2 crucibles is not yet clear. The results imply that B_2O_3 with a high-moisture content can be used for growth of high-purity, undoped GaAs SiO_2 crucibles; however, as shown in Fig. 5, twinning associated with growths using high OH-content

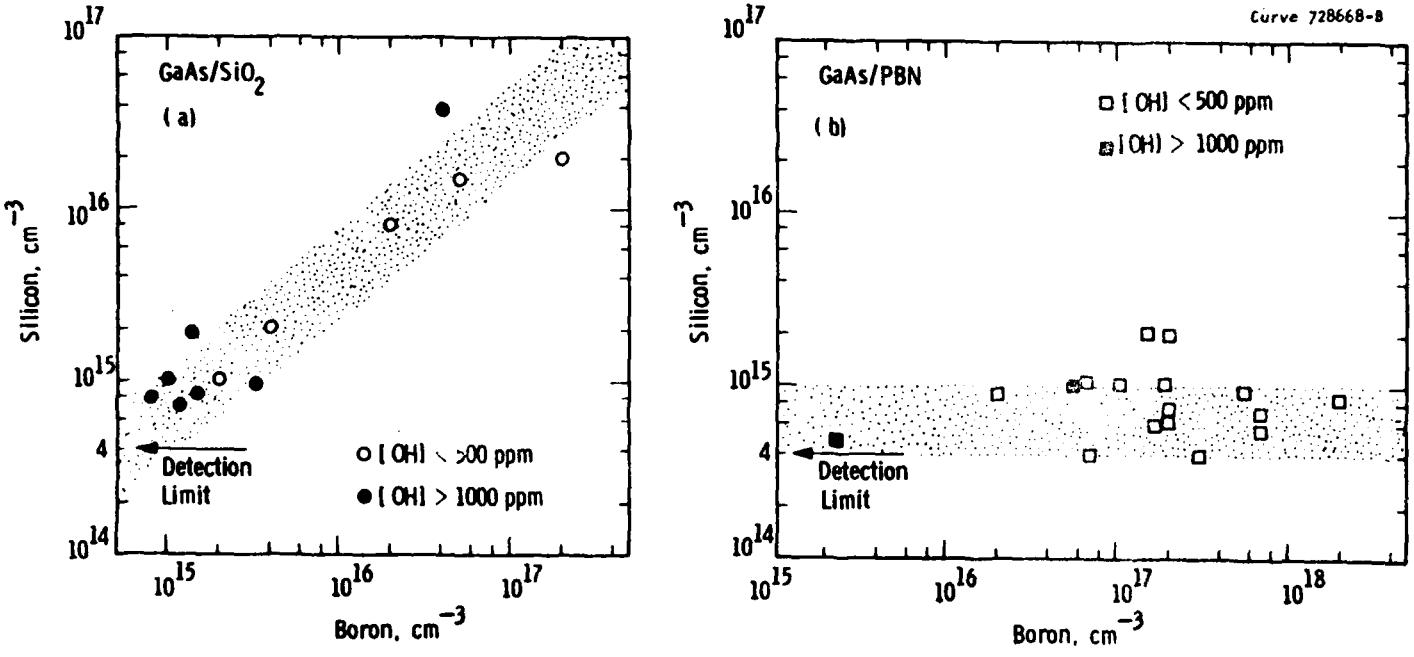

Figure 15 Effect of H_2O content in boric oxide encapsulant on silicon and boron incorporation in undoped LEC GaAs.

B_2O_3 makes this technique prohibitive for achieving reproducible growth of high-quality, large, semi-insulating single crystals of GaAs.

For growths of undoped GaAs crystals from PBN crucibles, silicon content is always near the detection limit of the SIMS instrument (~4 × 10^{14} cm^{-3}), while boron can range from low 10^{15} cm^{-3} up to 10^{18} cm^{-3}.

3.2 Impurity Content By Mobility Analysis

An alternative assessment of GaAs purity can be obtained from mobility measurements on as-grown substrates. Fig. 16 shows mobility measurements for a number of undoped GaAs/PBN and Cr-doped GaAs/PBN crystals using a high-impedance van der Pauw technique.[30] The substrates were prepared as outlined in Section 2.3. Van der Pauw samples were cavitroned from the wafer centers. After cleaning in trichloroethane and propanol, soldered indium ohmic contacts to the van der Pauw samples are formed. Mobilities ranging from 5000 to 7000 cm^2/vsec are typical of undoped GaAs/PBN and are consistent with a total ionized impurity concentration in the 1 × 10^{16} cm^{-3} range as determined using a Brooks-Herring analysis.[31] Comparison with the Brooks-Herring theory at $n \simeq 10^6$ to 10^7 cm^{-3} should be valid for semi-insulating GaAs with n-type conduction. To get approximate consistency for Cr-doped GaAs, an assumption is made that the Cr is doubly ionized.

These measurements indicate that undoped GaAs/PBN material contains residual ionized impurities in the 1 × 10^{16} cm^{-3} range and suggest that boron in GaAs/PBN crystals does not contribute significantly to ionized impurity scattering. However, the role of boron as a deep-level impurity or its interaction with native defects to form a low residual concentration of electrically active complexes cannot be entirely ruled out. Therefore, the mechanism by which the boron is incorporated is of interest. As shown in Fig. 17, Ga is the predominant impurity in the B_2O_3 after growth (as determined by emission spectrographic analysis). It is speculated that the reaction of Ga with the boron nitride crucible at the GaAs growth temperature (1238°C) gives

Curve 728130-A

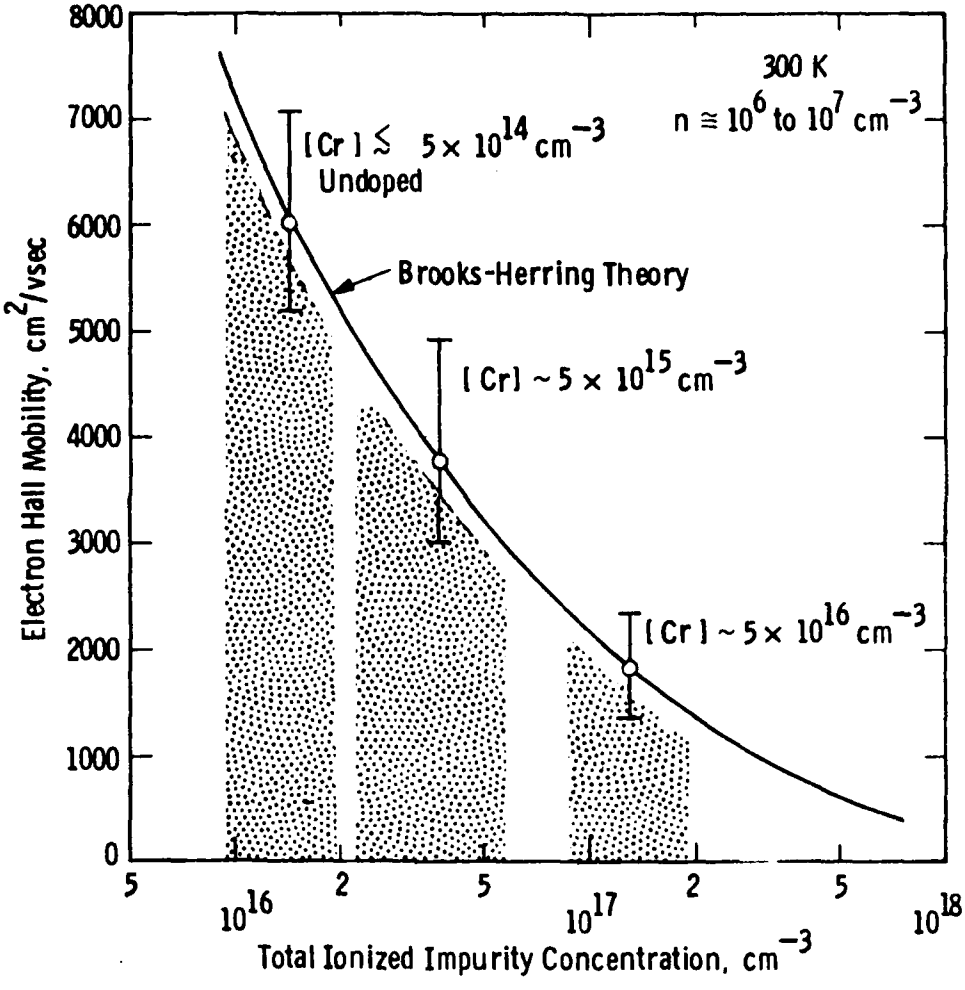

Figure 16 Apparent mobility vs. total ionized impurity content for n-type semi-insulating GaAs.

Curve 728663-A

Boron Incorporation in GaAs/PBN:

1) $BN + Ga \xrightarrow{1200°C} GaN\uparrow + B$

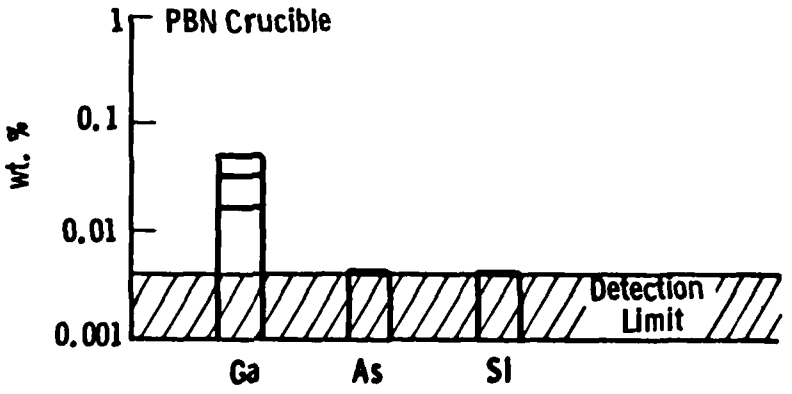

Figure 17 Analysis (in wt %) of impurities in B_2O_3 after crystal growth from PBN and quartz crucibles.

rise to sufficient boron in the GaAs melt to account for the observed SIMS concentrations. Investigations are continuing on the exact role of boron in GaAs crystals pulled from PBN crucibles.

4. ELECTRICAL CHARACTERIZATION

Resistivity and thermal stability measurements have been carried out on LEC-grown GaAs substrates to determine the suitability of the substrates for ion implantation studies. Table III shows the results of resistivity measurements on substrates representative of GaAs crystals pulled from pyrolytic boron nitride crucibles and, for comparison, quartz crucibles. The substrates were taken from near the crystal shoulder unless indicated otherwise. Substrate resistivities in the mid-10^8 ohm-cm range are observed in conventionally Cr-doped substrate material (containing mid-10^{16} cm^{-3} Cr concentrations) pulled from quartz crucibles compared to resistivities of mid-10^7 ohm-cm in undoped GaAs/PBN crystals ($< 5 \times 10^{14}$ cm^{-3} Cr content) and resistivities of 10^8 ohm-cm observed in lightly Cr-doped GaAs/PBN crystals (mid-10^{15} cm^{-3} Cr content). In contrast to other work,[32] undoped GaAs crystals pulled in our laboratories from fused-silica crucibles show lower resistivities and exhibit large seed to tang variations from crystal to crystal, ranging from 10^6 to 10^7 ohm-cm in one to resistivities as low as 0.09 ohm-cm range in another crystal, even though the crystals exhibit SIMS impurity concentrations roughly equivalent to those observed in GaAs pulled from pyrolytic boron nitride crucibles.

Thermal stability of substrates for ion implantation was assessed by means of resistivity measurements following an encapsulated anneal of the semi-insulating slice (prior to implantation) to determine whether any conducting surface layers formed as a result of thermal treatment. Samples for the unimplanted, encapsulated anneal test were prepared using the same plasma-enhanced silicon nitride capping process as is used for implantation (see Section 5). The encapsulated wafers were annealed at 860°C for 15 minutes in a forming gas atmosphere. Surface sheet resistances exceeding 10^6 ohms/□ are desired after

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TABLE III – RESISTIVITY MEASUREMENTS ON SUBSTRATES† REPRESENTATIVE OF GaAs CRYSTALS PULLED FROM PYROLYTIC BORON NITRIDE AND QUARTZ CRUCIBLES

Chromium Content (cm^{-3})	As-Grown Resistivity (Ω cm)	As-Grown R_s (Ω/□)	Post-Implant Anneal R_s (Ω/□)
LEC/PBN			
Undoped (5e14)	7e7	1.2e9	1.4e7
	6e7	5.3e9	1.3e7
	4.8e7	4.3e8	9e7
5e15	2e8	3.1e9	4.1e8
	1.7e8	4.0e9	4.5e7
LEC/QTZ			
Undoped (5e14)	3e7 tang	7.7e8	$\ll 10^6$[b]
	9e5	2e7	–
	2.5e3	6.1e4	–
	0.09	–	–
	0.35	–	–
5e16	5.8e8	1e10	1.4e9
	3.9e8	1.2e10	4e9
	5.7e8	1.2e10	7e8

[a] Si_3N_4 Capping and 860°C/15 m Annealing.

[b] FETs and monolithic circuits fabricated on these substrates found to exhibit excessive leakage.

† Samples are from near crystal shoulder unless otherwise specified

annealing to ensure isolation of passive, as well as active elements in analog IC processing.

Typical sheet resistance data for semi-insulating undoped and lightly Cr-doped ($< 5 \times 10^{15}$ cm^{-3}) GaAs/PBN substrates as well as undoped and conventionally Cr-doped ($> 1 \times 10^{16}$ cm^{-3}) GaAs substrates before and after encapsulated anneals are shown in Table III. Some degradation in the sheet resistance was always observed as a result of the thermal treatment, but the leakage currents measured in the low field measurements (10^3v/cm) and the rf losses observed in monolithic circuits fabricated on these substrates were low. In particular, surface leakages of <30 μA at 15 volts bias and high breakdown voltages of 25 volts were measured in interdigitated capacitor structures (5 μm separation and 13.2 mm periphery) to test the performance under the high operating fields normally utilized in monolithic circuits.[33]

4.1 Axial Resistivity Uniformity

Figures 18, 19, 20, and 21 show resistivity measurements for as-grown LEC GaAs crystals as a function of crystal length (or equivalently, the fraction of melt solidified, g) for undoped GaAs/PBN, undoped GaAs/SiO_2, and GaAs/PBN to which small amounts of Cr were added. Measurements were made from the seed end of the crystal (g = 2 to 7%) to the last to freeze (tang) portions of the crystals (typically g = 90 to 95%).

4.1.1 GaAs Crystals Pulled From PBN Crucibles

The undoped GaAs/PBN (Fig. 18) crystals demonstrate reproducibly high, semi-insulating behavior from seed to tang with resistivity ranging from mid-10^7 ohm-cm to 10^8 ohm-cm and mobilities ranging from 4800 to 6800 cm^2/sec. The greatest nonuniformity for this material occurs only in the last 10% of the melt solidified (e.g., see the data for WBN-23); however, no low-resistivity behavior ($< 10^6$ ohm cm) has as yet been observed even in the last-to-freeze sections of these

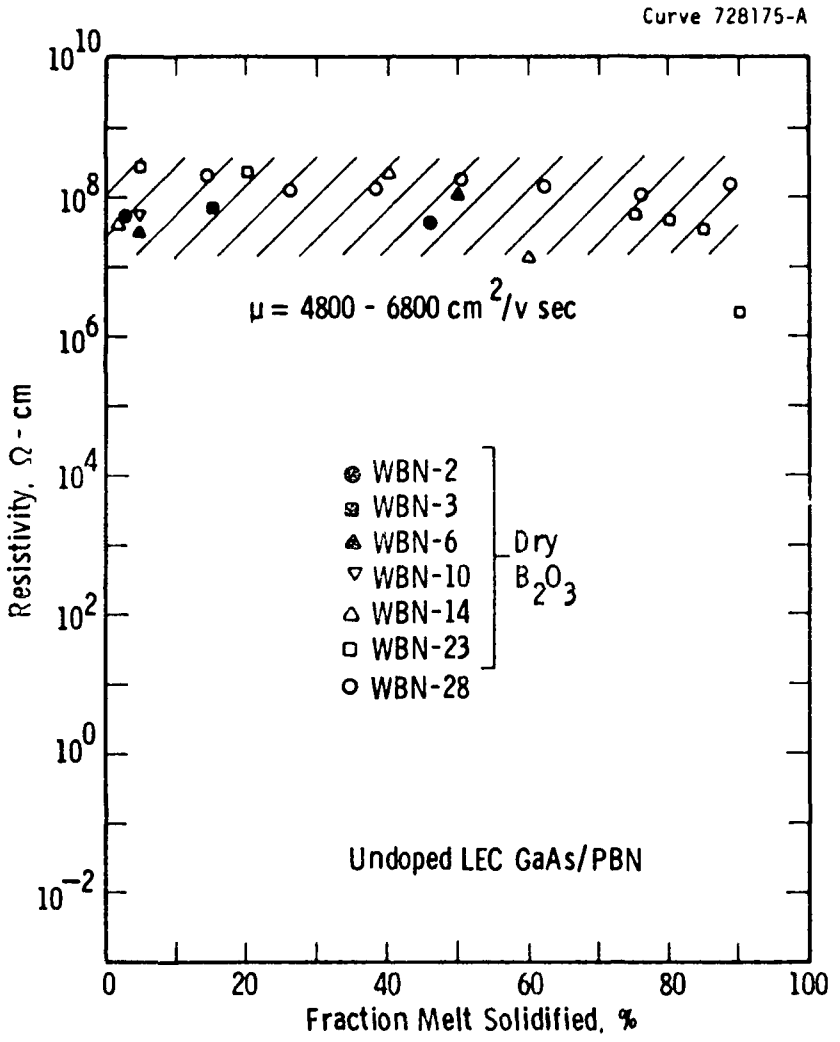


Figure 18 Axial resistivity variation of undoped LEC GaAs pulled from PBN crucibles.

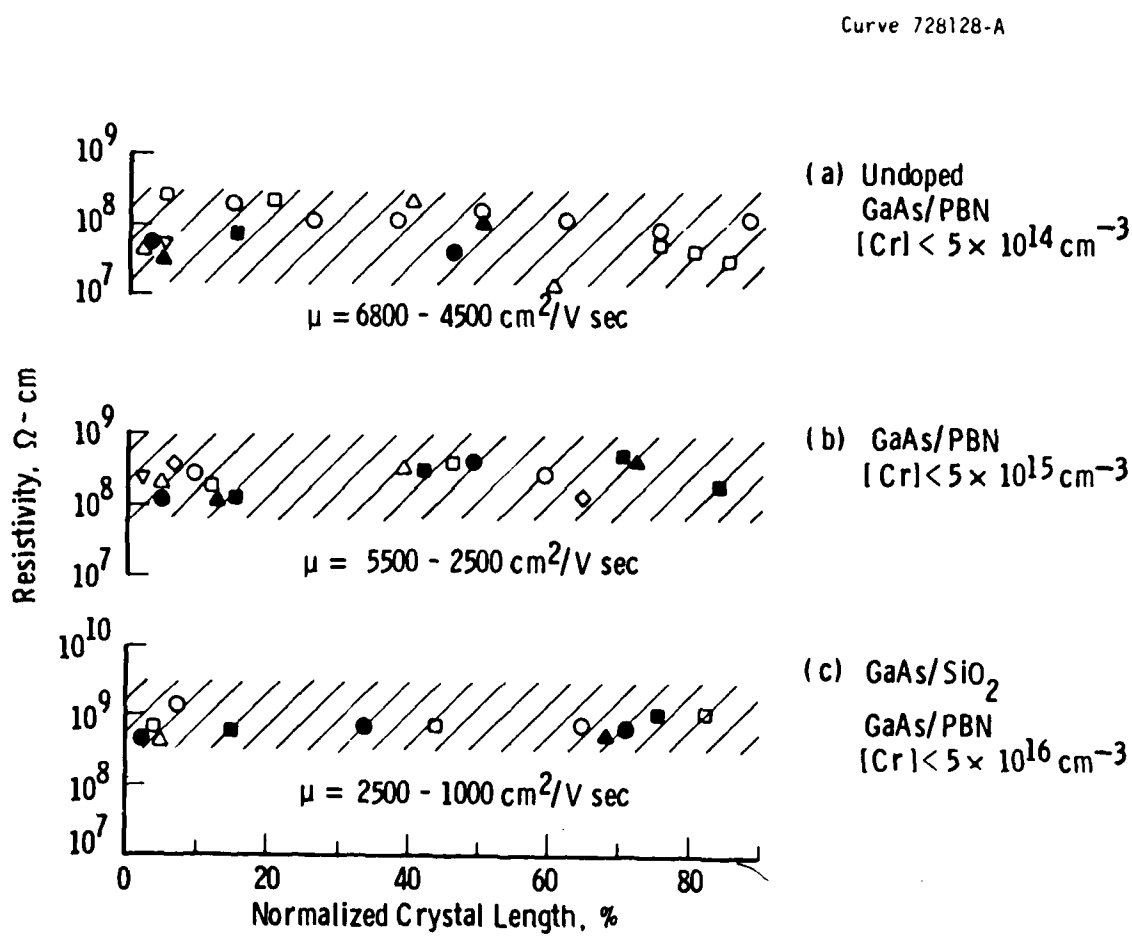


Figure 19 Axial resistivity variation in GaAs/PBN crystal as function of chromium doping.

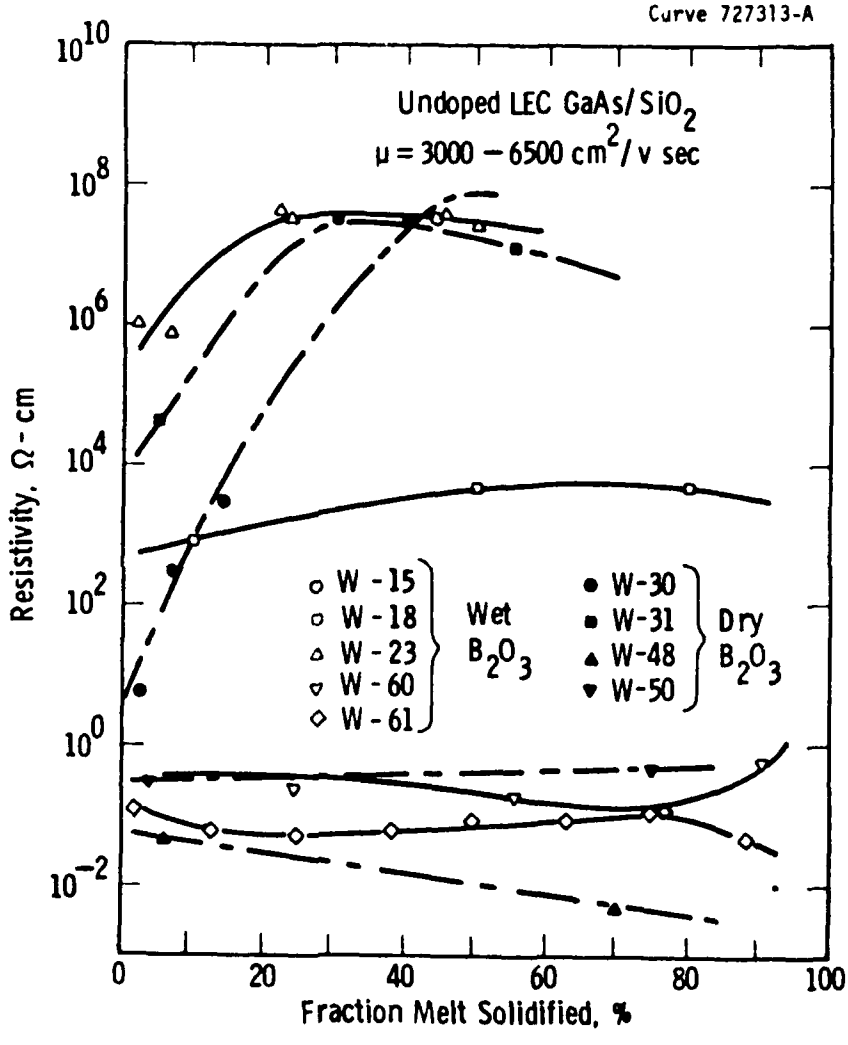


Figure 20 Axial resistivity variation of undoped LEC GaAs pulled from SiO_2 crucibles.

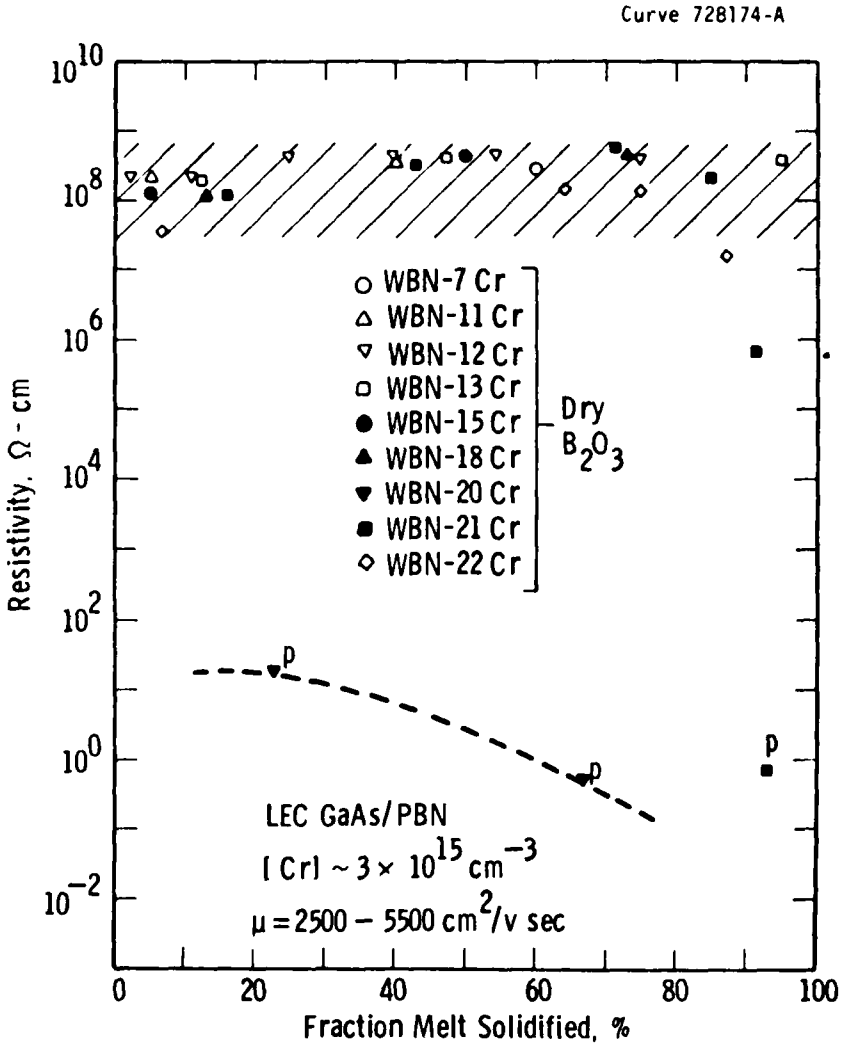


Figure 21 Axial resistivity variation of Cr-doped LEC GaAs pulled from PBN crucibles.

unintentionally doped ingots. Additions of small amounts of chromium ($< 5 \times 10^{15}$ cm^{-3}) result in a slight increase of resistivity as shown in Fig. 19 and a corresponding reduction in mobility. These results suggest that high Cr concentrations in GaAs/PBN substrates serve no useful purpose and contribute to excessive ionized impurity scattering, as well other detrimental effects related to impurity redistribution.[34,35]

4.1.2 GaAs Crystals Pulled From Fused SiO_2 Crucibles

In marked contrast to the undoped GaAs/PBN results, undoped crystals pulled from SiO_2 containers (shown in Fig. 20) yield material with highly variable and unpredictable resistivities from seed to tang, and the crystals are highly non-reproducible from run to run. This variability in resistivity persists regardless of the pre-growth moisture content of the B_2O_3 used. The data of Fig. 20 can be divided into two sets corresponding to growths using vacuum-baked "dry" B_2O_3 (closed points, $[H_2O]$ = 300 to 500 ppm wt) and "wet" B_2O_3 (open points, $[H_2O]$ = 1000 to 5000 ppm wt). In order to vary the moisture content in a controlled way, 5-inch diameter, 600-gm, vacuum-baked disks of B_2O_3 were cleanly cracked into small pieces to maximize the surface area. The B_2O_3 was then allowed to absorb moisture from the atmosphere at normal temperature and pressure while the total weight of the B_2O_3 was monitored. In this way, boron oxide with a pregrowth $[H_2O]$ content between 300 to 5000 ppm wt was produced. Growths W-15, W-18, and W-23 used B_2O_3 with a pregrowth moisture content of ~1000 ppm wt. Large fractions of these crystals exhibit low-resistivity behavior. For growths W-60 and W-61, a pregrowth moisture content of 3270 ppm wt (W-60) and 5000 ppm wt (W-61) were used. For both growth runs the crystal pulling was not begun until a holding period of 50 hrs had transpired from synthesis and melt-down. It has been speculated that such a holding period prior to the actual crystal pull would allow the B_2O_3 to accomplish any "gettering" of impurities from the melt. However, this procedure of using a high-moisture content B_2O_3 together with a holding period for "gettering" was not successful in producing undoped, semi-

insulating GaAs pulled from SiO_2 crucibles. Both W-60 and W-61 growths yielded low-resistivity, n-type material from seed to tang with carrier concentrations in the mid-10^{15} cm^{-3} to mid 10^{16} cm^{-3} range.

The growths consisting of W-18, W-48, W-50, W-60, and W-61 are also illustrative of LEC growths of unintentionally doped GaAs crystals pulled from different types of fused-silica containers. Crystals W-18, W-60, and W-61 were pulled from conventional fused-silica crucibles (GE HV-214), while W-48 and W-50 were pulled from ultra high-purity synthetic fused-SiO_2 containers. W-48 was pulled from a low-water-content synthetic (Suprasil-W, 5-10 ppm wt OH); W-50 was pulled from a high water-content synthetic (Spectrasil, 1500 ppm wt OH). All of these crystals exhibited low resistivity, n-type behavior regardless of the water content of the crucible material or of the B_2O_3 encapsulating layer.

4.1.3 Lightly Cr-Doped GaAs/PBN

Figure 21 shows axial resistivity data for Cr-doped GaAs pulled from PBN crucibles. Small amounts of chromium were added to the melt as a compensating impurity (1 to 5 × 10^{15} cm^{-3}). The as-grown resistivities of these crystals ranged from low-10^8 ohm-cm at the seed to mid-10^8 ohm-cm (tang) and are somewhat higher than for the undoped GaAs/PBN material of Fig. 18. In only two out of 25 growths of GaAs from PBN crucibles has any anomaly in the semi-insulating behavior been observed. One growth (WBN-20 Cr) exhibited anomalously low-resistivity, p-type behavior over the whole crystal length, 14 ohm cm seed end (g = 23%) to 0.5 ohm-cm progressing toward the tang end (g = 70%). The carrier concentration ranged from 1.6 × 10^{15} cm^{-3} to 3.7 × 10^{16} cm^{-3} with mobilities of 300 cm^2/vsec. This behavior indicates the presence of a segregating acceptor impurity having a relatively shallow energy level. However, the exact nature of the impurity is not known. Variable temperature Hall-effect analysis for a sample taken at a point g = 27% (Fig. 22) shows a slope corresponding to an activation energy of 0.027

Curve 727772-A

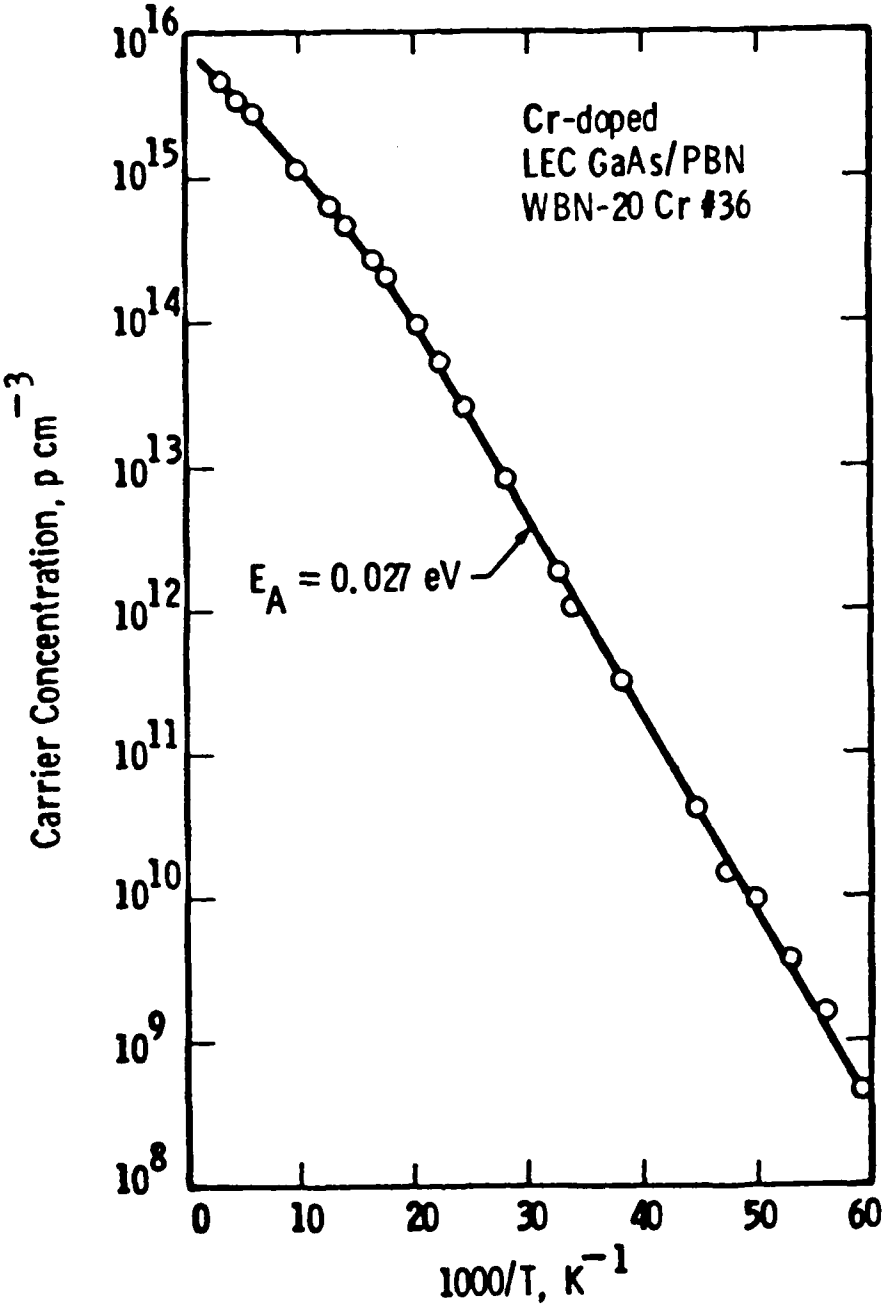


Figure 22 Carrier concentration vs. reciprocal temperature for anomalously p-type Cr-doped LEC GaAs pulled from PBN crucible, g = 27%.

eV. This energy level is close to reported shallow energy levels for Cu (0.023 eV) and Zn (0.026 eV) in GaAs,[36] although the large concentration (10^{16} cm^{-3}) observed at exhaustion in Fig. 22 is difficult to reconcile with impurities such as Cu having fractional distribution coefficients, since several mgms of dopant would have to be inadvertently added to the melt to achieve a concentration of 10^{16} cm^{-3} in the solid.

Hall-effect data for a low-resistivity, p-type tang-end sample (g = 93%) from WBN-21 Cr are shown in Fig. 23. This sample was taken from the last-to-freeze portion of the crystal and showed an activation energy of 0.079 eV with a concentration at exhaustion of mid 10^{16} cm^{-3}. SIMS analysis of p-type samples from WBN-20 Cr and WBN-21 Cr exhibited no large quantities of impurities $> 10^{15}$ cm^{-3} except for Cr (3 to 5 $\times$ 10^{15} cm^{-3}) and boron (1×10^{17} to 1×10^{18} cm^{-3}). Swiggard et al.[37] have also observed a similar p-type behavior in last-to-freeze portions of small (< 200 gm) undoped GaAs ingots pulled from PBN containers. They attribute the behavior to Cu contamination, based on a Hall-effect analysis yielding an activation energy of 0.14 eV. However, their identification of the impurity was somewhat inconclusive, and they did not rule out the possibility of an acceptor-like point-defect complex.

4.2 Radial Resistivity Uniformity

In Fig. 24 resistivity is plotted as a function of position along the wafer diameter for a Cr-doped GaAs/SiO_2 (curve b) and an undoped GaAs/PBN substrate (curve c). Also, we show a typical plot of dislocation density as a function of normalized radius. The coincidence of the maxima and minima in the data support a model in which, in the case of the Cr-doped sample, a fraction of the chromium preferentially segregates to regions of high-dislocation density (center and edge) where it precipitates out in the areas of high-defect density and thereby becomes electrically inactive, resulting in a slight reduction in resistivity in these regions.

Curve 727770-A

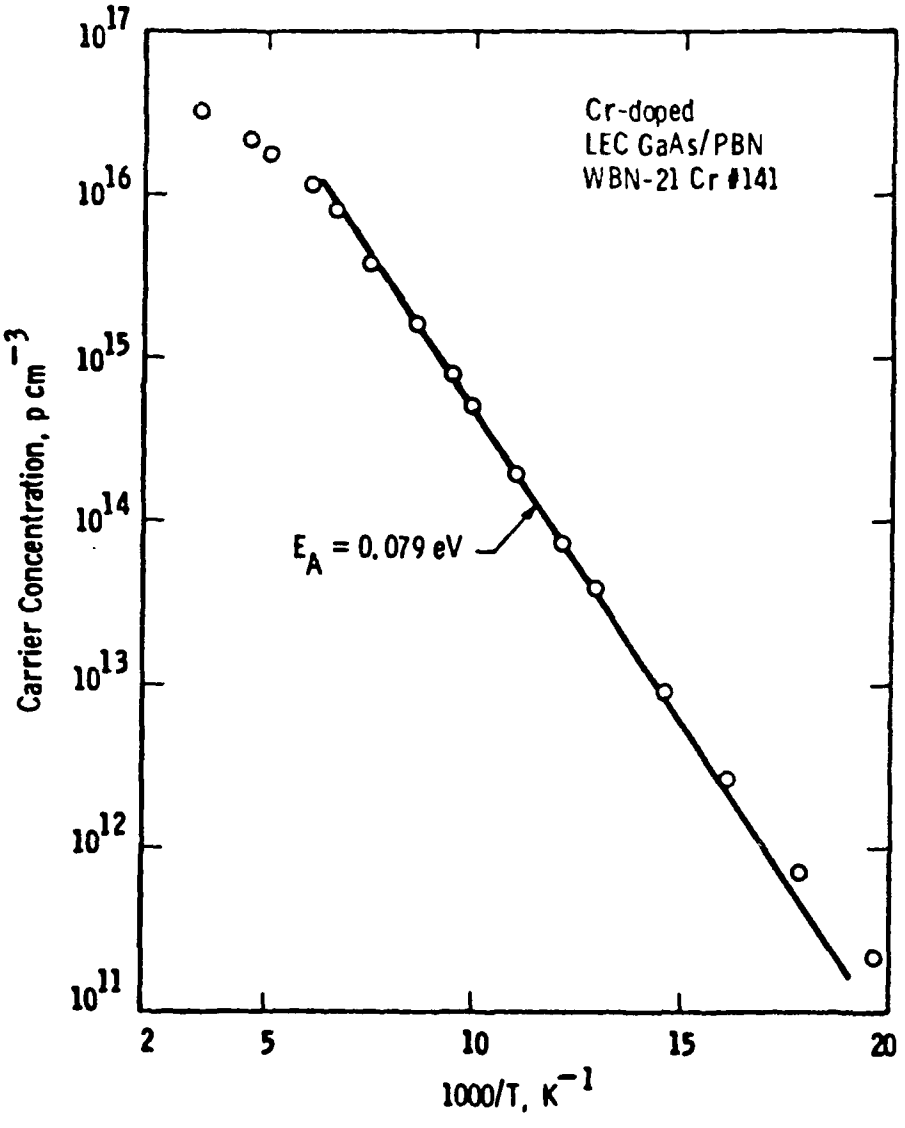


Figure 23 Carrier concentration vs. reciprocal temperature for anomalously p-type Cr-doped LEC GaAs/PBN sample taken from last-to-freeze portion of ingot. g = 93%.

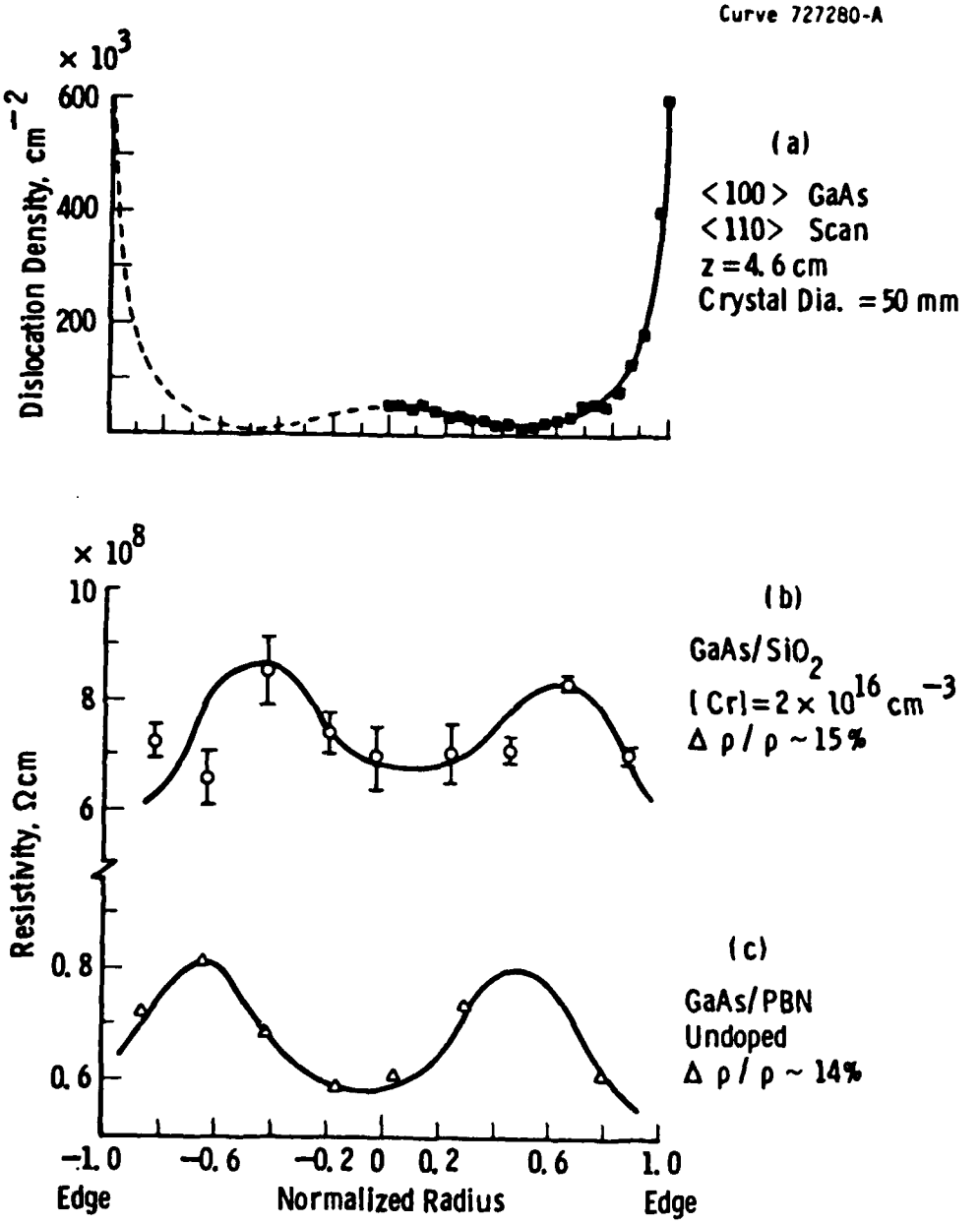


Figure 24 Resistivity vs. position along substrate dia. compared to dislocation density variation.

A model for the resistivity variation of the undoped GaAs/PBN material is less clear but probably involves the radial distribution of the deep-donor defect level (e.g., EL2), which is believed to dominate the semi-insulating behavior of this material. Martin et al.[38] have obser by IR techniques a systematic radial variation in the concentration of EL2 similar to that observed for the dislocation density. They attribute the systematic radial distribution of EL2 to the presence of stresses which affect the density of lattice-point defects during growth of the bulk LEC material.

4.3 Axial Mobility Uniformity

High-impedance van der Pauw measurements[30] have been used to assess the axial mobility uniformity of as-grown LEC GaAs crystals pulled from PBN and fused-SiO_2 crucibles. Fig. 25 shows Hall mobility measured on as-grown substrates as a function of normalized crystal length for several undoped, semi-insulating GaAs/PBN crystals. Mobilities range from 4500 to 7000 cm^2/vsec over the full crystal length up to 90%. The mobility typically tends to fall below 4000 cm^2/vsec in the tang-end portions of these ingots, owing to impurity segregation and increased ionized impurity scattering in last-to-freeze sections of these crystals.

4.4 DLTS Measurements

Preliminary investigations into the effect of thermal heat treatments on the density of deep levels in LEC GaAs have been carried out. To probe deep levels associated with the bulk substrate material, the DLTS measurements were performed by standard transient capacitance techniques using aluminum Schottky ring-dot structures fabricated directly on the as-grown and annealed samples. Figs. 26b and 27b show DLTS spectra typical of as-grown LEC GaAs material. In both spectra the major electron trap is due to the 0.81 eV level (normally denoted as the EL2 level), a deep-donor level, which typically occurs with a mean density of $\sim 10^{16}$ cm^{-3} in LEC bulk GaAs.[38]

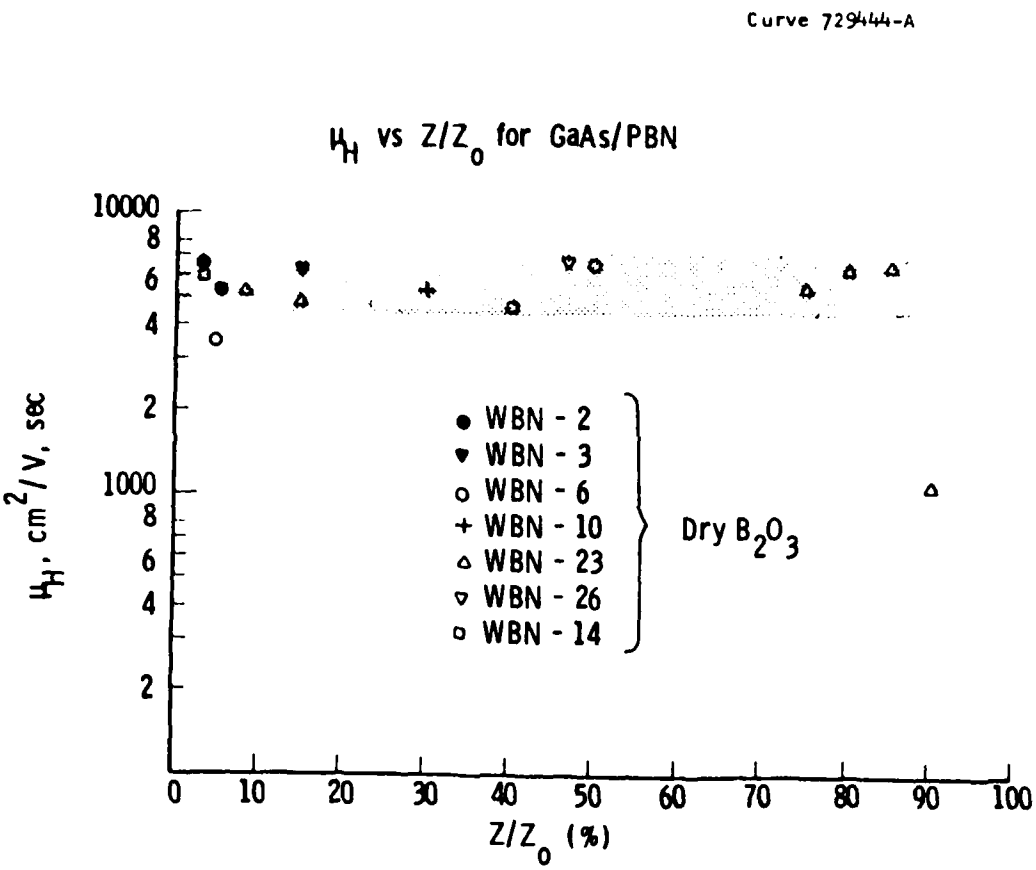


Figure 25 Axial variation of apparent electron mobility for undoped LEC GaAs crystals pulled from PBN crucibles.

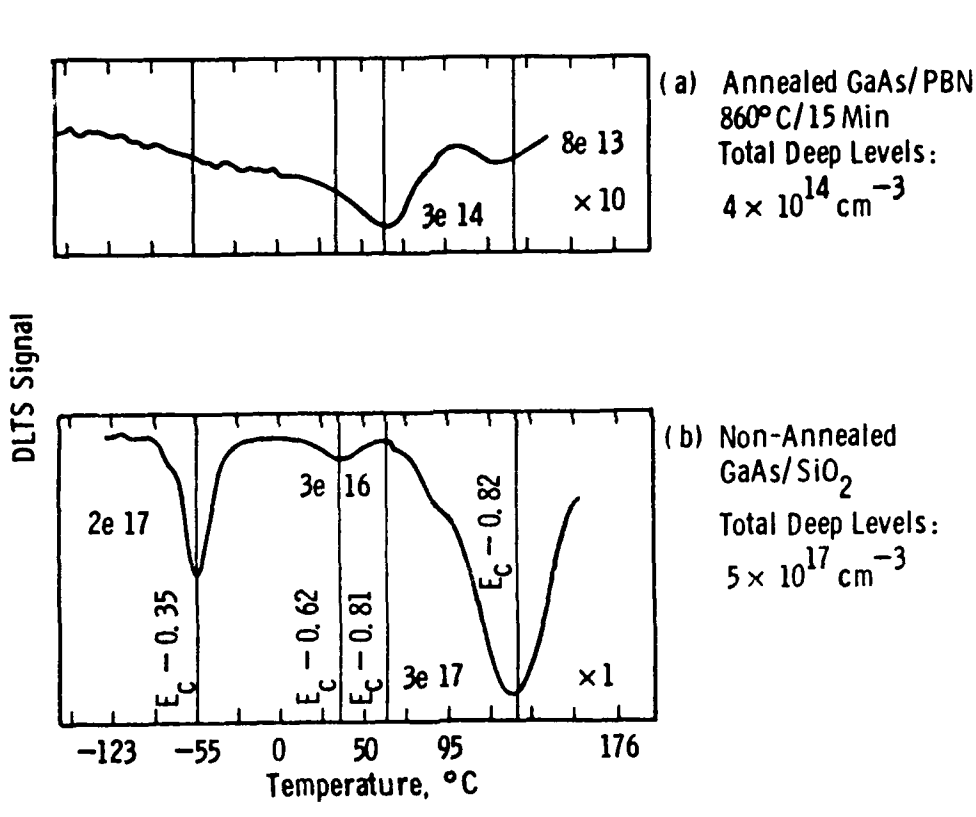


Figure 26 Effect of 860°C/15-min anneal on deep levels in LEC GaAs.

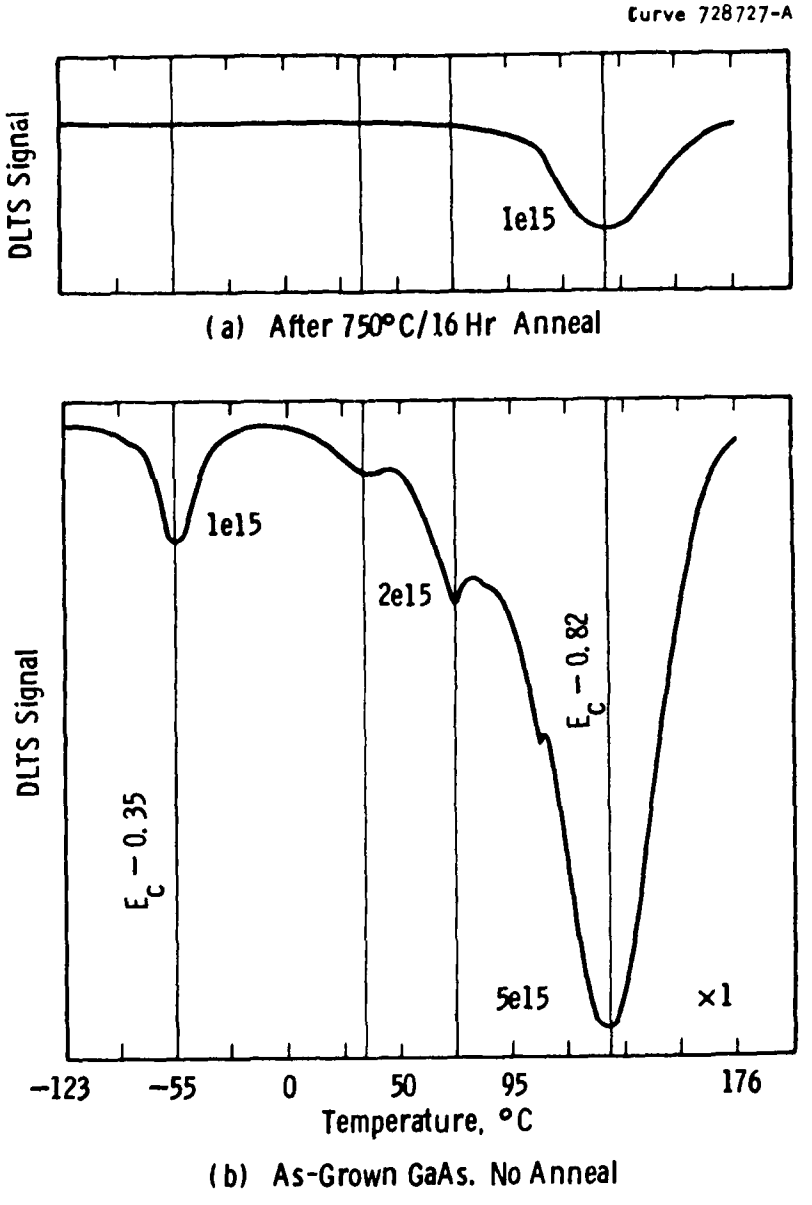


Figure 27 Effect of 750°C/16-hr. anneal on deep levels in LEC GaAs.

The importance of the deep-donor level observed directly in DLTS measurements of Figs. 26 and 27 in controlling the semi-insulating behavior of GaAs is supported by the results of Fig. 28, where Arrhenius plots of log resistivity are presented as a function of reciprocal temperature for undoped and Cr-doped LEC GaAs crystals pulled from PBN and fused-SiO_2 crucibles. All the samples showed conduction by electrons to be dominant and independent of the Cr-content up to 8×10^{16} cm^{-3}. An activation energy of 0.76 eV was measured for all sample types and reflects the presence of the deep-donor EL2 level in all of these materials.

The exact nature of the EL2 level is as yet unclear, and two models have been put forward to account for its presence in LEC GaAs: (1) the EL2 level is due to oxygen in GaAs or at least related to the presence of oxygen in GaAs[39]; (2) EL2 is a complex lattice defect, the creation of which is probably connected with the presence of stresses during the course of cystal growth.[38] Recent observations of Martin et al.[40] indicate that there is no clear dependence of the concentration of the deep donor EL2 on the concentration of oxygen in Bridgman-grown GaAs crystals. If the EL2 level is related to native point defects in the crystal, its concentration may be proportional to the amount of nonstoichiometry present in the as-grown solid. Thus, the density of this deep level should be influenced by thermal effects such as long-duration low-temperature anneals (< 950°C) since, based on the phase extent of GaAs solid, the compound rapidly approaches the stoichiometric composition at temperatures below ~950°C.[41]

In Fig. 26a, DLTS measurements are shown for an undoped GaAs/PBN sample which was capped with Si_3N_4 and direct ion implanted using $^{29}Si^+$ ions to form an active n-layer of $\sim 1 \times 10^{17}$ cm^{-3} peak doping. The capped sample was then exposed to a standard implantation anneal of 860°C for 15 min. For a net doping density of 1×10^{17} cm^{-3} the detection limit of the DLTS technique is 1×10^{13} cm^{-3}. Over the range of temperatures investigated (-123°C to 176°C), the undoped GaAs/PBN sample (Fig. 26a) displays a total density of deep levels of 5×10^{14}

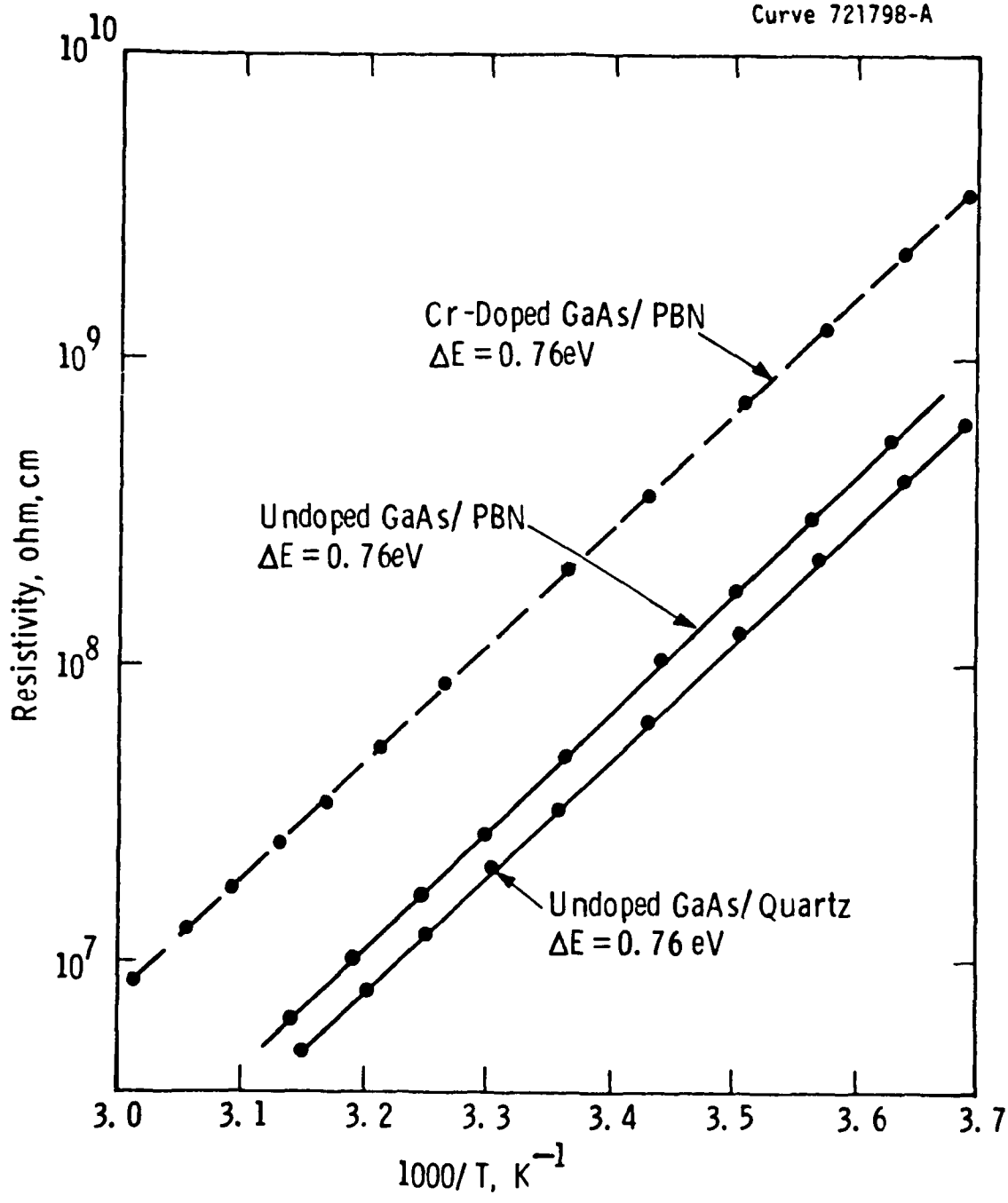


Figure 28 Log resistivity as a function of reciprocal temperature for LEC GaAs grown in PBN and SiO_2 crucibles.

cm^{-3}, a factor of 100 to 1000 lower density than observed in typical as-grown LEC GaAs material.

These studies have been extended to longer anneal times at lower temperatures as shown in Fig. 27. The data correspond to a 500-micron thick polished GaAs/SiO_2 substrate (W-60, #4; ρ = 0.3 ohm-cm, n = 5 × 10^{15} cm^{-3}), one-half of which was exposed to a 16-hr, 750°C anneal in arsenic overpressure (Fig. 27a), while the other half served as a nonannealed, as-grown control sample. Aluminum Schottky ring-dot structures were fabricated directly on the as-grown polished substrate surface. Annealed samples were repolished to remove approximately 12.5 microns of surface. Aluminum Schottky ring-dot structures were then deposited on this polished surface. For a net doping density of 5 × 10^{15} cm^{-3}, the detection limit of the DLTS technique is 5 × 10^{11} cm^{-3}. Over the range of temperatures investigated (-123°C to 176°C), the total density of deep levels in the as-grown material (Fig. 27b) is 1 × 10^{16} cm^{-3}, with the dominant trap being the EL2 (0.82 eV) level having a concentration of 5 × 10^{15} cm^{-3}. After a 16-hr anneal at 750°C in an arsenic overpressure (Fig. 27a), the total deep-level density is reduced to 1 × 10^{15} cm^{-3} with the shallower traps being entirely removed. On the basis of the work of Mircéa, et al.[42] on the outdiffusion of deep electron traps in epitaxial GaAs (taking a diffusion coefficient for EL2 of D = 10^{-6} cm^2/sec at 750°C and an as-grown [EL2] concentration of ~1 × 10^{16} cm^{-3}), the diffusion profile for [EL2] across a 500-micron thick wafer after a 16-hr anneal has a maximum of ~1 × 10^{15} cm^{-3} in good agreement with the observed concentration of deep levels exhibited by the DLTS spectrum corresponding to the 750°C anneal of Fig. 27a.

These annealing studies imply that the thermal history to which the crystal or substrates are exposed in the course of growth and processing can have a dramatic effect on the point-defect equilibrium and the resulting concentration of deep levels in the material.

5. DIRECT ION IMPLANTATION STUDIES

The object of the ion implantation studies has been to develop and demonstrate a reproducible implantation technology for semi-insulating GaAs substrates that will yield predictable, high quality, directly implanted n-layers. Intermediate tasks include:

- establish essential characterization procedures for directly implanted power FETs that simultaneously provide data on implant and substrate quality;
- develop scientific models of ion implantation characteristics of GaAs to provide the logical foundation required to meet yield and reproducibility objectives;
- provide feedback to crystal growth as required to optimize substrate technology.

In this section, we describe the application of surface Hall-effect measurements at ambient temperature for:

1. providing crystal-to-crystal implantation calibration for power FET preparation;
2. clarifying the physics involved in activation of implanted n-layers in GaAs;
3. crystal-to-crystal reproducibility and the effects of Cr doping on implantation response through mobility data;
4. demonstrating 100% activation of implanted ^{29}Si and estimating residual ionized impurity densities;
5. illustrating differences in activation characteristics resulting from Cr doping and suggest thermodynamic models of the observed response.

Based on prior work in the published literature, the implantation of n-layers into Cr-doped GaAs has resulted in a general belief that modeling of the activation of these layers would require knowledge of:

1. the particular species implanted;
2. the density and distribution of these species and its redistribution during anneal;
3. encapsulant-GaAs interface interaction and its effect on gettering of residual impurities and implanted species redistribution;
4. slice-to-slice and across-the-slice variations in residual impurity concentration;
5. annealing temperature and the exact annealing cycle;
6. encapsulant "quality" and resulting stoichiometry of the GaAs;
7. Cr distribution in the as-grown GaAs and the physics of the Cr, implanted species, and encapsulant interface interaction,

among other variables. This results in the pessimistic view that quoted results apply only to special qualified crystals and particular implantation, encapsulation, and annealing technologies. It must be assumed, therefore, that these quoted results cannot be transferred or reproduced. The objective of this discussion is to present evidence showing that n-implantation of undoped LEC GaAs/PBN can be reduced to a single variable problem. This variable is the implanted ion density. The complexities associated with Cr redistribution and interaction have been eliminated by removing Cr from the as-grown semi-insulating substrate. Residual impurity complications are eliminated through a significant reduction in this density and reproducible crystal growth to the same residual impurity density. Encapsulant integrity remains as a vital consideration, but preliminary results indicate that significantly different encapsulation technologies will yield equivalent results using these undoped GaAs/PBN substrates. Preliminary results also indicate that the annealing temperature is not a critical variable, and that the

changes associated with a change in annealing temperature can be understood using simple thermodynamic models. This demonstration of the simplicity and reproducibility of undoped LEC GaAs/PBN response is complemented by a discussion of LEC Cr-doped GaAs showing systematic differences in response at both low and high implanted-ion densities, which can be correlated to Cr doping density. The effect of Cr at typical densities required for FET channels has been discussed in the attached publications, (see Appendix).

Of necessity, almost all of the data presented here refer to wafers implanted and annealed using a specific, fixed technology. This technology has been discussed in the attached publications; it is reviewed here for the readers' convenience.

The semi-insulating substrates are (100) wafers with <110> orientation flats cut from ground and flatted <100>-grown LEC crystals. These wafers are bromine-methanol front surface polished, back surface etched, and approximately 0.020 inches thick. A 900 Å front surface Si_3N_4 encapsulation deposition initiates implantation processing. This nitride is deposited at 340°C at a rate of 70 Å per minute using plasma-enhanced reaction of SiH_4 and N_2. Nitride deposition is followed by deposition of 2500 Å of phosphosilicate glass. Conventional photolithography and ion milling of the phosphosilicate glass is employed to define selective, direct implantation of the semi-insulating substrates. The photoresist-glass composite is used as the beam stop for ambient temperature implantation through the 900 Å Si_3N_4 encapsulant. Implantation is performed at 7° misalignment using the $^{29}Si^+$ or $^{29}Si^{++}$ beams generated using a SiF_4 ion source in a 400 kV ion implanter. Penetration of the Si_3N_4 layer and machine voltage limit the implantation energy range to 100 keV and 800 keV, respectively. All implantations are performed at multiple energies and doses calculated to approximate flat ^{29}Si chemical profiles having effective thicknesses of 0.15 to 0.75 microns with respect to the Si_3N_4-GaAs interface.

Implantation is followed by deposition of 2500 Å phosphosilicate glass layers on both front and back surfaces which act as secondary encapsulation. Annealing is performed at 860°C for 15 min in flowing forming gas. Profiling of the activated layers is performed using front surface Schottky barrier aluminum metallization for capacitance profiling. Hall samples are prepared in a van der Pauw configuration using either selective implantation or mesa isolation. Alloying of ohmic contacts to these Hall samples is performed with the Si_3N_4 retained in the field area. The Hall measurements are performed at 300°K and 77°K using magnetic fields of 1300 to 5300 gauss.

5.1 Implantation Characterization and Power FET Technology

The following equations act as a guide in the design and analysis of n-layers implanted for power FET channels.

$$N_{SM} = \int_{\lambda d} n(z)dz \tag{1}$$

$$I_{fc} = qN_{SM}\, v_{sat} \tag{2}$$

$$V_{SDB} \approx \gamma\, V_B(n)\, [\, 1 - (N_{SM}/N_{SMO}(n))^2] \tag{3}$$

where z is the depth with respect to the as-implanted surface, λ_d, is the surface depletion depth, n(z) is the free carrier or net donor profile, and N_{SM} is the undepleted concentration per unit area measured with respect to the as-implanted surface. The full channel current (I_{fc}) of gate-recessed FETs is related to N_{SM} through the saturation velocity (v_{sat}) (Eq. 2). The source to drain breakdown voltage (V_{SDB}) (Eq. 3) of these FETs is related to N_{SM} through the concentration per unit area [$N_{SMO}(n)$] that could be depleted at this volume concentration (n) at the breakdown voltage $V_B(n)$ in an ideal parallel-plate geometry, and a

numerical factor, $\gamma \sim 3$. These equations lead to an estimate of optimum N_{SM} for maximum power and the output load line for maximum power.

Profiling n(z) followed by numerical integration to obtain N_{SM} is found to lack the precision required to specify doses for channel implants or to assess the reproducibility of activation. Profiling is useful, however, to confirm that calculated, flat ^{29}Si implantation profiles result in flat net donor activity profiles. Typical profiles for ^{29}Si implants through Si_3N_4 encapsulating layers into semi-insulating GaAs grown from PBN crucibles are shown in Fig. 29. These profiles are in good agreement with the calculated ^{29}Si distribution and show net activation efficiencies of 70 to 85%.

Surface Hall-effect measurements yield undepleted concentration per unit area according to:

$$N_{SMH} = [\int_{\lambda d} \mu(z)n(z)dz]^2 / \int_{\lambda d} \mu^2(z)n(z)dz \qquad (4)$$

$$\mu_{SH} = \int_{\lambda d} \mu^2(z)n(z)dz / \int_{\lambda d} \mu(z)n(z)dz \qquad (5)$$

which is very precise and accounts for surface depletion correctly, although it systematically underestimates N_{SM} by 5 to 10% as a result of the Hall factor and depth averaging for typical, flat FET profiles shown in Fig. 29. Measurements of I_{fc} versus N_{SMH} yield $v_{sat} = 1.23 \pm .05 \times 10^7$ cm/sec independent of profile width, low field mobility, and consistent with the expected underestimate. From this perspective, the control of n required for reproducible FET input characteristics is a consequence of N_{SM} and effective profile width control. The effective profile width is controlled by the highest energy implant. Implantation of a number of specimens at fixed maximum energy and scaled total dose results in a crystal-by-crystal calibration of N_{SMH} versus total dose. Typical data for lightly Cr-doped GaAs/PBN substrates are shown in Fig. 30. Similar data for undoped GaAs/PBN substrates are included

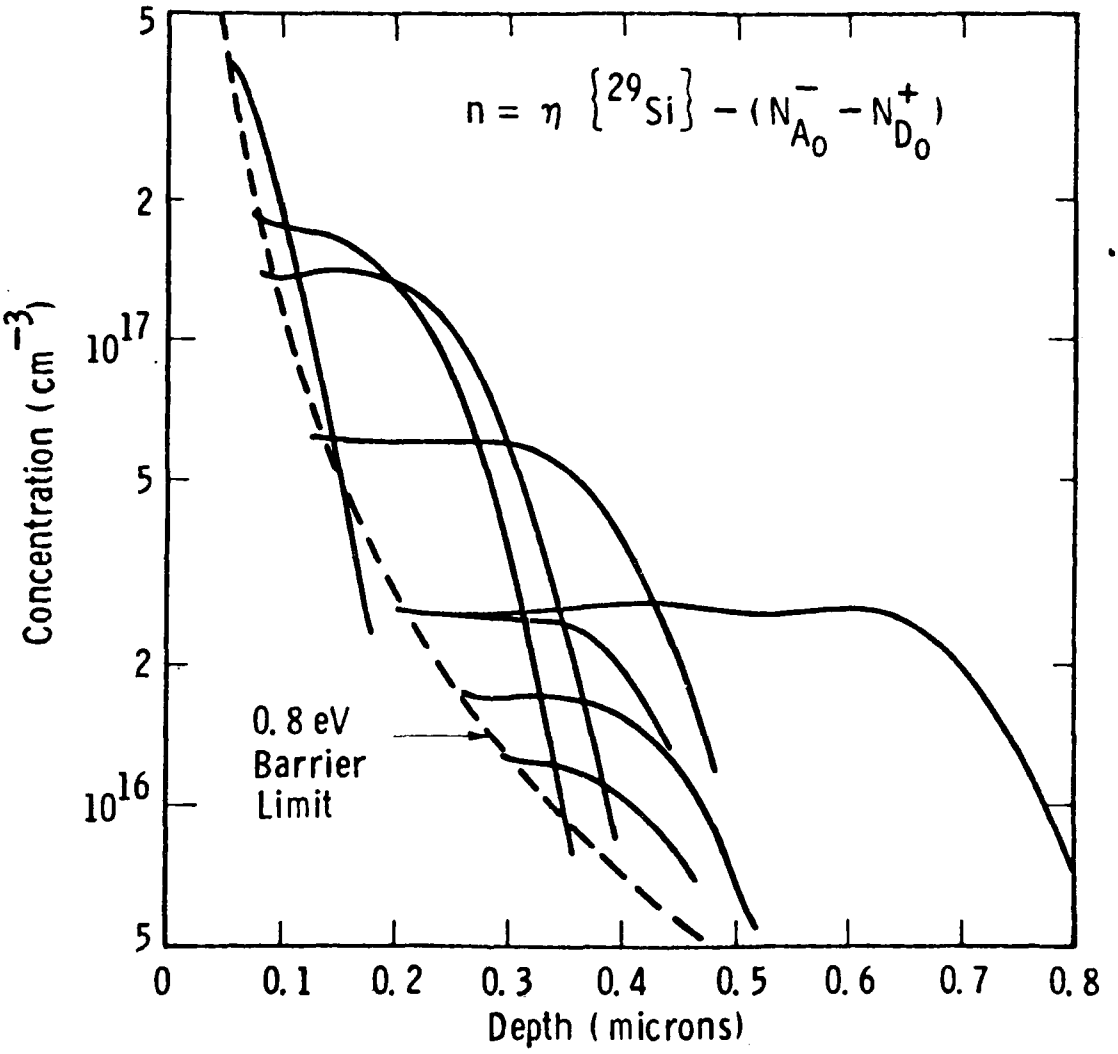


Figure 29 Typical net donor implantation profiles showing a "flat" activity from a "flat" implanted ^{29}Si distribution.

Curve 728920-A

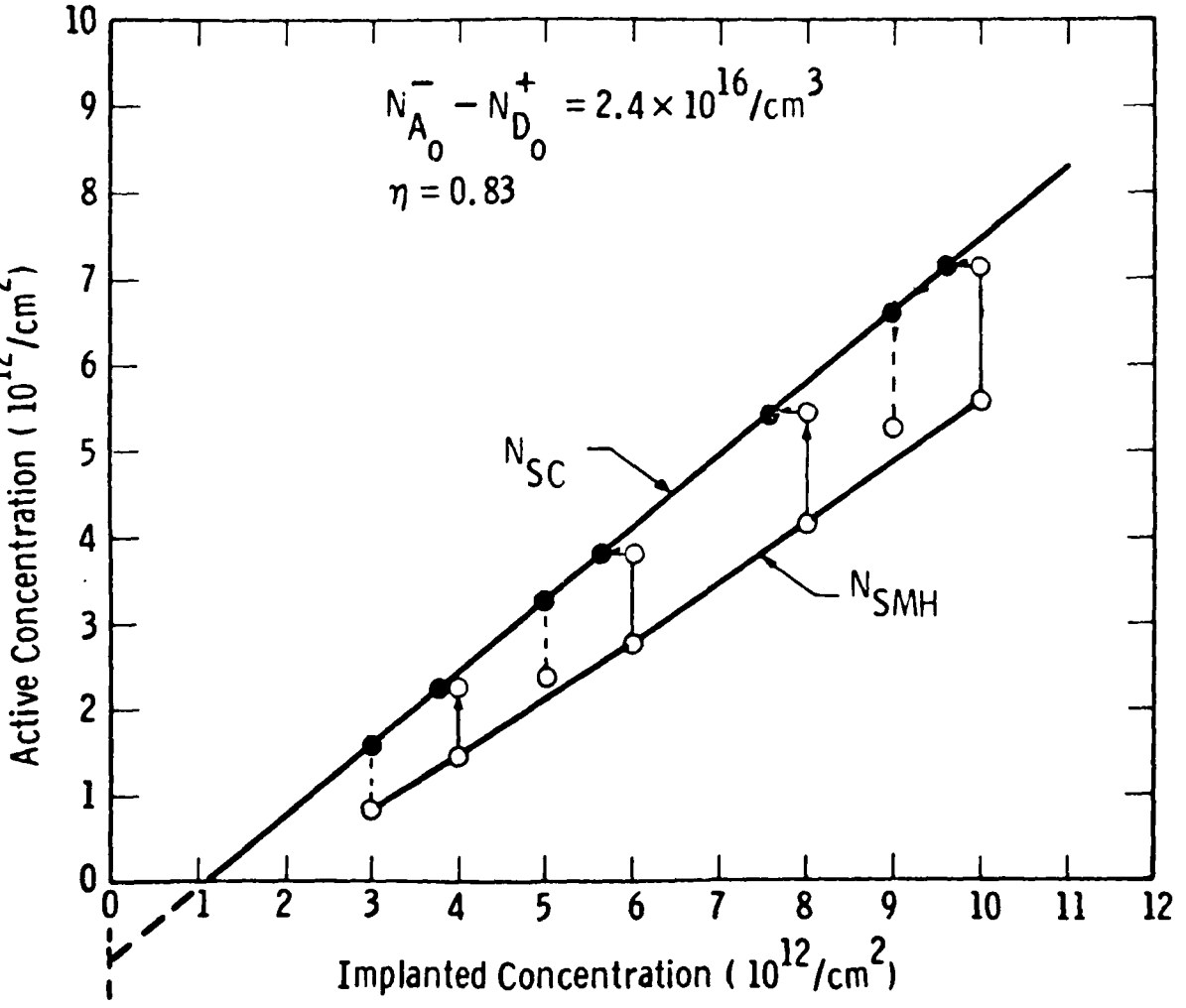


Figure 30 Typical activation calibration for power FET channel implantation. Data corrected to permit calculation of differential activation efficiency.

in the attached publications. The measured data allow interpolation of the dose required to achieve a desired undepleted concentration cm^{-2} at this channel width. For GaAs crystals pulled from PBN crucibles, the reproducibility from crystal-to-crystal required to achieve $N_{SMH} = 2.4 \times 10^{12}$ cm^{-2} is $5.6 + 0.2 \times 10^{12}$ cm^{-2}, which corresponds to a variation of ± 3.5%. A meaningful activation efficiency figure can be obtained only after correcting N_{SMH} for surface depletion and correcting the Si dose for deposition in the Si_3N_4 encapsulating layer. The slope of the corrected data yields the differential net donor activation efficiency, while the activity intercept divided by the effective profile width yields the net density of acceptor levels ($N_{A_o}^- - N_{D_o}^+$) that must be filled to raise the Fermi level to the conduction band edge.

5.2 Total Activation of Implants into GaAs

Electrical activity measurements made on ion-implanted n-layers in semi-insulating GaAs cannot be related directly to the implanted ions. Correspondence between the implanted concentration and the measured net activity, reproducibility from wafer-to-wafer and crystal-to-crystal, and similarity in the implanted chemical profile and net donor profile suggest only that the measured activity must be associated with electrical activity of the implanted species itself. There are no direct measurements that can resolve the possible electrical roles of implanted ^{29}Si as substitutional donors, substitutional acceptors, substitutional donor-vacancy pairs with acceptor character, substitutional donor-acceptor pairs, and inactive interstitials[43] or substrate-related reaction products that could contribute to the readily measured net activation. This limitation has not been directly addressed in the past, and substrate preparation and implantation variables have been modified to achieve 100% net donor activation. The tacit assumption has been made that this would correspond to complete utilization of the implanted species with negligible contribution from the substrate. This assumption is totally erroneous and, if used in the present case of GaAs/PBN material, it would constitute a particularly

significant error since only 70 to 85% net donor activation efficiency has actually been observed in implantation in GaAs/PBN crystals grown by the LEC technique.

Resolving the electrical activity due to implanted species and the contribution due to the substrate is a primary objective of this program. It should be noted that n-type GaAs can be achieved by S, Se, Te, Si, Ge, and Sn doping of the crystal during LEC growth, liquid-phase epitaxy, vapor phase epitaxy, or ion implantation; however, there are no reliable data to show 100% donor activity of any of these dopants under any particular growth condition. Although the amphoteric doping possibilities of the Group IV dopants are obvious, the Group VI dopants can also result in partially compensated doping by mechanisms which are not understood. It is essential then to analyze implantation activation from the perspective of total activation efficiency η_Σ

$$\eta_\Sigma = d(N_D^+ + N_A^-)/d\{^{29}Si\} = d\Sigma/d\{^{29}Si\} \qquad (6)$$

where Σ is the total density of ionized impurities, and $\{^{29}Si\}$ is the concentration of implanted silicon. Σ can be obtained from mobility data at 77°K or ambient temperature if it is recognized that errors will occur when the implanted layer is so defective that ionized impurities no longer dominate scattering, neutral donor-acceptor pairs will not be detected, and multiple charged centers or complexes will contribute as the square of the charge state.[44,45,46] $\eta_\Sigma < 1$ may imply:

1. incomplete activation;
2. outdiffusion of the implanted species;
3. pairing with residual impurities at low concentrations;
4. self-pairing at high concentrations;

while $\eta_\Sigma > 1$ may imply:

1. unannealed radiation damage;
2. substrate decomposition;

3. encapsulant failure;
4. residual impurity gettering.

Reports in the literature which claim ~100% net donor activation imply η_Σ = 1.5 to 2.5 in all cases. Since only half of the activity is associated with the implanted species itself, a reproducible, transferable technology cannot be assumed. The correct objective is η_Σ = 1 so that, for example,

$$\Sigma = N_D^+ + N_A^- = \{^{29}Si\} + N_{D_o}^+ + N_{A_o}^-$$

can be written where $N_{D_o}^+$ is the residual shallow donor density, $N_{A_o}^-$ is the total residual acceptor density, and these additive constants can be related to the measured impurity content of the as-grown crystal.

The quality of the net activation is then defined in terms of an internal net activation efficiency, η_Δ

$$\eta_\Delta = d(N_D^+ - N_A^-)/d(N_D^+ + N_A^-)$$

$$= d\Delta/d\Sigma \qquad (8)$$

which can be derived from Hall data on a series of samples. η_Δ directly reflects the amphoteric doping character as a function of substrate type, implant species, and annealing temperature.

Equations (6) and (8) provide an analytical method for investigating both the implantation of n-layers in semi-insulating GaAs substrates and the substrates themselves. These activation efficiency variables η_Δ and η_Σ are technology-oriented variables of the implantation process and are related to the free carrier concentration and implanted concentration through

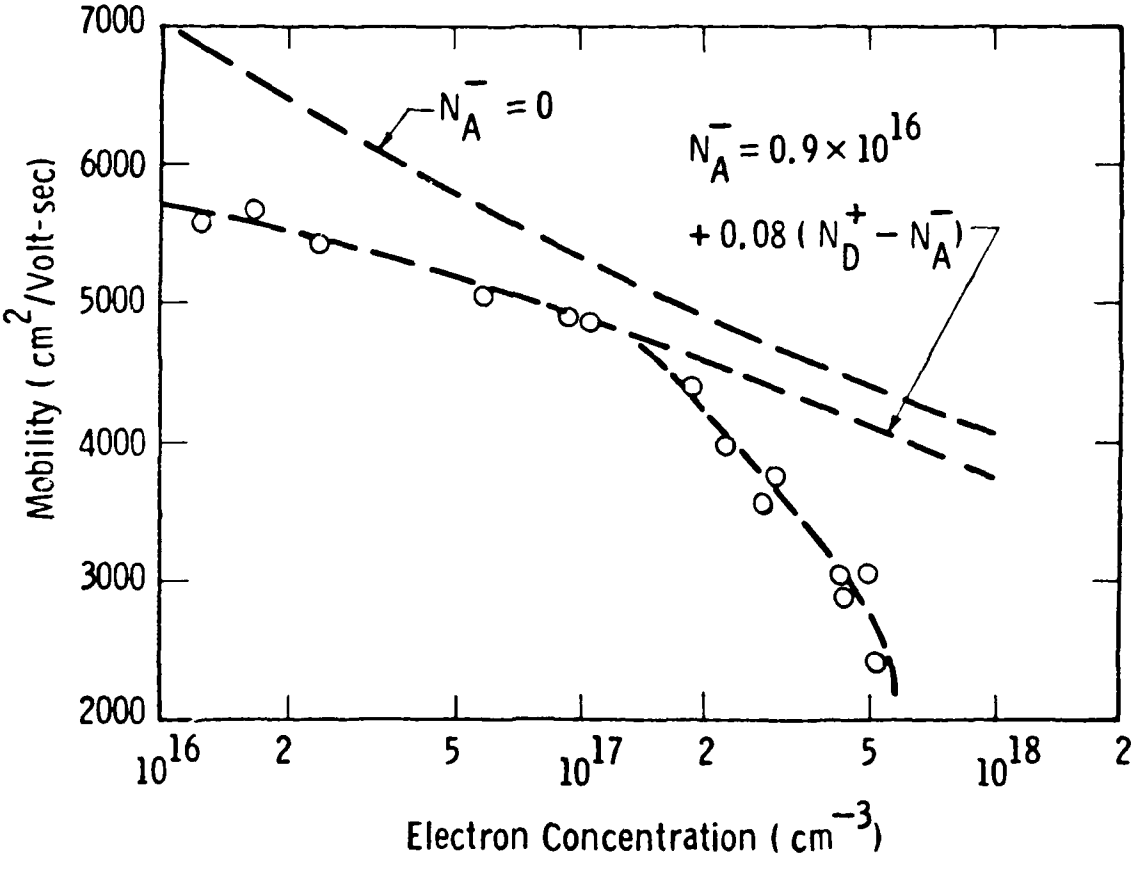
$$n = (N_D^+ - N_A^-) = \int_o \eta_\Delta \eta_\Sigma \, d\{Si\} - (N_{A_o}^- - N_{D_o}^+) = \eta\{Si\} \qquad (9)$$

5.3 Mobility Characteristics of Si Implanted LEC GaAs Substrates

Figure 31 shows ambient temperature μ_{SH} values as a function of $\Delta = N_D^+ - N_A^-$ for undoped GaAs crystals grown from PBN crucibles. Each data point corresponds to values obtained from a "flat" profile implant of ^{29}Si through a Si_3N_4 cap followed by 860°C annealing. Each data point corresponds to a separate wafer selected at random for $g \lesssim 0.80$ (where g is the fraction of melt solidified) from any of four typical undoped crystals. Approximately 10% of the accumulated data is included to indicate typical scatter. Fig. 31 includes data from implanted layers of different thicknesses; implanted layer thickness is not a significant variable. Bare implantation of ^{29}Si followed by Si_3N_4 encapsulation results in equivalent data so that the implantation and encapsulation sequence cannot be considered significant. Limited data obtained using controlled atmosphere anneals at 860°C suggest similar behavior and that the encapsulation is not a significant variable either. (This does not imply that inferior encapsulation will not lead to mobility reductions and a significant deviation from the characteristic presented in Fig. 31.) Finally, more extensive data on controlled atmosphere anneals at 760°C and on encapsulated anneals at 960°C yield two new characteristics where the differences can be rationalized in terms of the different annealing temperatures. It can be concluded that the characteristic shown in Fig. 31 is a consequence of the thermodynamics of Si activation in undoped GaAs/PBN at 860°C and typical residual impurity densities in these crystals. It is not the result of the particular wafer or crystal or of specialized, subconscious processing details that cannot be reproduced or transferred.

Selected theoretical data from Walukiewicz et al.[44] is laid over the data in Fig. 31 to aid in preliminary analysis. First, it is clear that the theoretical limit of an uncompensated n-layer is not achieved. This could only occur if the implanted Si appeared only in donor or electrically inactive states and there were no acceptors in the as-grown material. Second, the mobility at low concentrations can be attributed to $N_{A_o}^- = 0.8$ to 1.0×10^{16} cm^{-3} residual acceptor centers, a

Curve 728923-A



... at 300°K as a function of electron concentration for ... SI, LEC GaAs/PBN wafers implanted with $^{29}Si^+$.

value comparable to the residual Mn + Mg + C concentrations detected by SIMS in these crystals. The activation threshold for this material is also $(N_A^- - N_D^+) \sim 0.8 \times 10^{16}$ cm^{-3} suggesting that $N_D^+ \lesssim 0.2 \times 10^{16}$ cm^{-3}. This value is comparable to the Si + S concentration detected by SIMS. Third, the compensation ratio rises rapidly beyond $\Delta = 1.5 \times 10^{17}$ cm^{-3}, suggesting an amphoteric doping behavior which is dependent upon the concentration of implanted Si. Finally, the increase in compensation ratio suggests that it may not be possible to achieve $(N_D^+ - N_A^-) \gtrsim 6 \times 10^{17}$ cm^{-3} in undoped GaAs using Si implants and 860°C annealing.

Figure 32 shows ambient temperature μ_{SH} values as a function of $\Delta = N_D^+ - N_A^-$ for Cr-doped GaAs crystals (Cr $\lesssim 5 \times 10^{15}$ cm^{-3}) grown from PBN crucibles. Again, these data result from arbitrarily selected wafers from four different crystals doped with 2 to 5×10^{15} cm^{-3} Cr, and represents the activation of implanted Si in Cr-doped GaAs/PBN. This level of Cr doping results in a characteristic that is essentially identical to that of undoped substrates for 6×10^{16} cm^{-3} $< N_D^+ - N_A^- < 3 \times 10^{17}$ cm^{-3}. The low, erratic mobility values observed at lower concentrations can be attributed to the Cr itself since its doubly charged character affects $N_D^+ - N_A^-$ as -2 {Cr} and Σ as +4 {Cr} so that both $\Delta = N_D^+ - N_A^-$ and Σ become very sensitive to any Cr outdiffusion or pairing with implanted Si donors. It is shown in the following section that the Cr is present as doubly ionized acceptors for $\Delta < 5 \times 10^{16}$ cm^{-3} but cannot be detected at higher concentrations. Even though the Cr is not present as unpaired acceptors during measurement, its presence in the as-grown substrate or its presence in the implanted layer during the anneal itself is reflected in a substantial improvement in mobility for $\Delta > 3 \times 10^{17}$ cm^{-3}. This suggests that the Cr affects the amphoteric doping of implanted Si at higher concentrations.

Figure 33 shows ambient temperature μ_{SH} values as a fuction of $N_D^+ - N_A^-$ for Cr-doped GaAs crystals [Cr] $\lesssim 5 \times 10^{16}$ cm^{-3} pulled from fused-SiO_2 crucibles. The Cr doping level in this case is 2 to 6×10^{16} cm^{-3}. As in the preceeding figures, data was taken from four different crystals except that the wafers were selected subject to $g \lesssim 0.50$ (where

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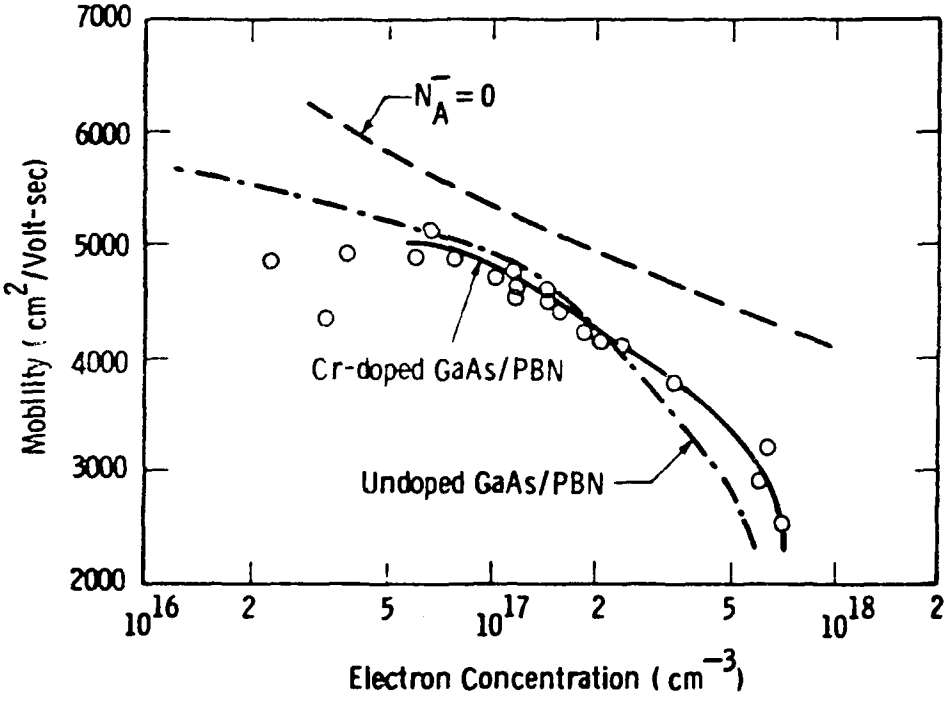

Figure 32 Mobility at 300°K as a function of electron concentration for lightly Cr-doped LEC GaAs/PBN wafers implanted with $^{29}Si^+$. [Cr] ~ 2 x 10^{15} cm^{-3}.

Curve 728922-A

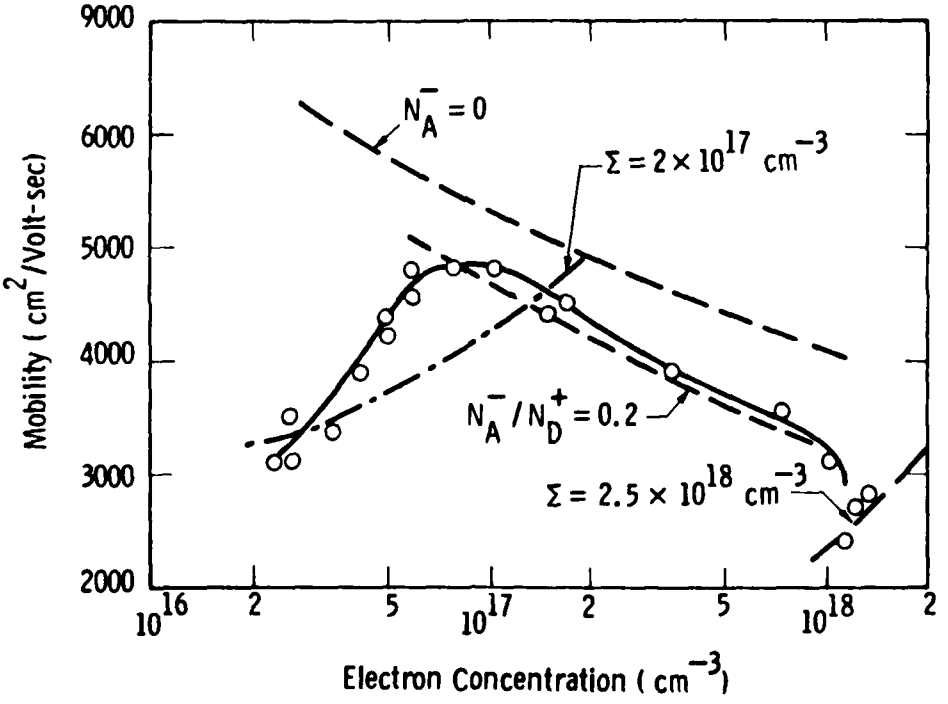

Figure 33 Mobility at 300°K as a function of electron concentration for moderately Cr-doped LEC GaAs/SiO_2 wafers implanted with $^{29}Si^+$. [Cr] ~ 5 x 10^{16} cm^{-3}.

g is the fraction of melt solidified). Consistent mobility values are achieved at concentrations as low as 3×10^{16} cm^{-3}, but comparison with theoretical mobility suggests an ionized-impurity concentration of 2 to 2.5×10^{17} cm^{-3} in this limit. This Σ value is attributed to 4 to 6 $\times$ 10^{16} Cr cm^{-3} which is doubly charged. Increasing the {Si} density to increase Δ then leads to a reduction in Σ which is associated with outdiffusion and pairing of the Cr. At Δ concentrations greater than 1.5×10^{17} cm^{-3}, Cr is no longer present as an isolated, ionized scattering center although its presence in the as-grown crystal and during the anneal results in further suppression of the amphoteric character of the implanted Si.

5.4 Total Electrical Activation of Silicon Implants in LEC GaAs Substrate

Figure 34 shows total ionized impurity concentration, $\Sigma = N_D^+ + N_A^-$ as a function of implanted {^{29}Si} for undoped GaAs/PBN substrates. This shows that all of the implanted Si is activated as singly ionized, isolated centers at all concentrations. Therefore, the increased compensation ratio at higher concentrations described previously is the result of a change in the amphoteric doping of the implanted Si itself, and not the result of spurious acceptor formation. At low implanted-Si concentrations there is some evidence of an additive constant $N_A^- + N_D^+ \approx 1.0 \times 10^{16}$ cm^{-3} corresponding to residual shallow donors plus residual acceptors, both of which must have levels such that they are ionized when $\Delta \gtrsim 2 \times 10^{16}$ cm^{-3}. The net activation data ($N_A^- - N_D^+$), the mobility data (N_A^-), and now the total activation data ($N_A^- + N_D^+$) yield a self-consistent model demonstrating that undoped LEC GaAs grown from PBN crucibles retains a residual impurity content of 1×10^{16} cm^{-3} throughout ion implantation processing.

Figure 35 shows Σ as a function of implanted {^{21}Si} for lightly Cr-doped (2 to 5 $\times$ 10^{15} cm^{-3}) GaAs grown from PBN crucibles. This again shows complete activation of the implanted Si. There is also some indication of saturation at the highest concentration, which could be attributed to formation of Si_{Ga}-Si_{As} nearest-neighbor pairs. The

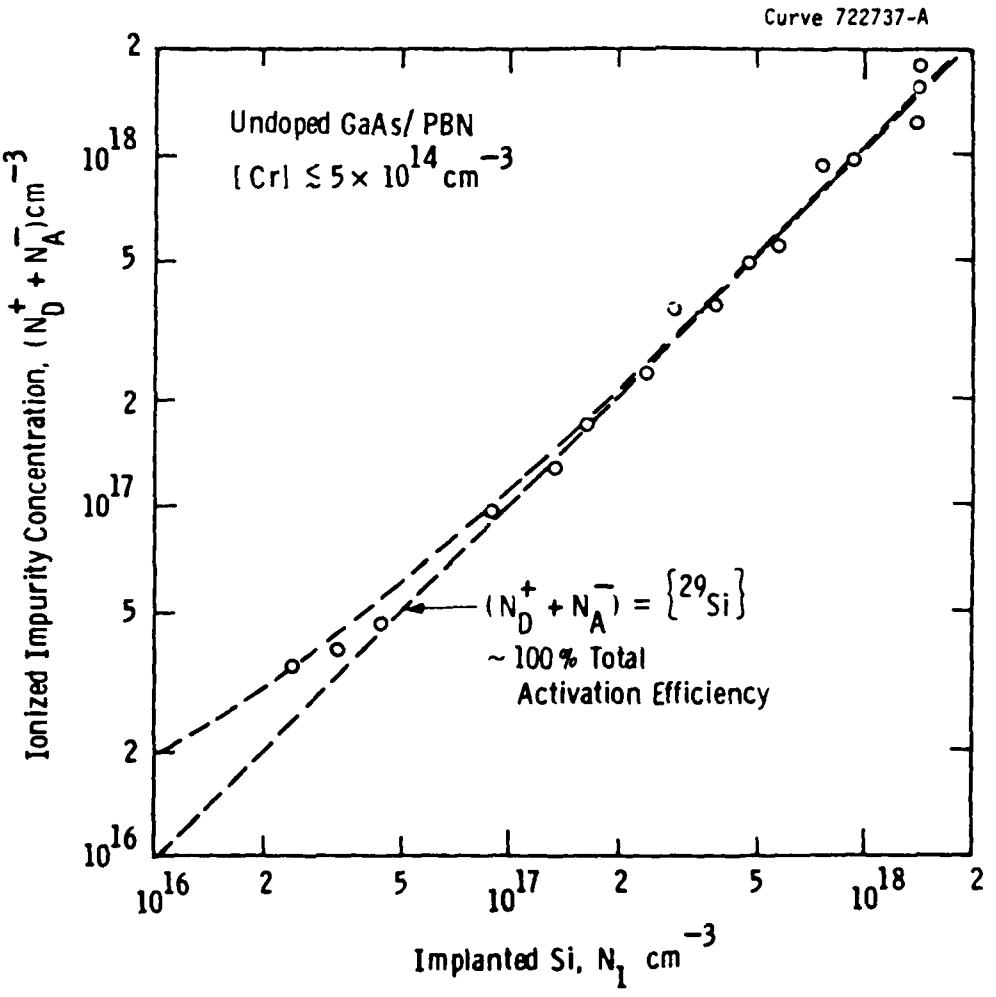

Figure 34 Ionized impurity density as a function of implanted ^{29}Si density for undoped LEC GaAs/PBN.

Curve 728925-A

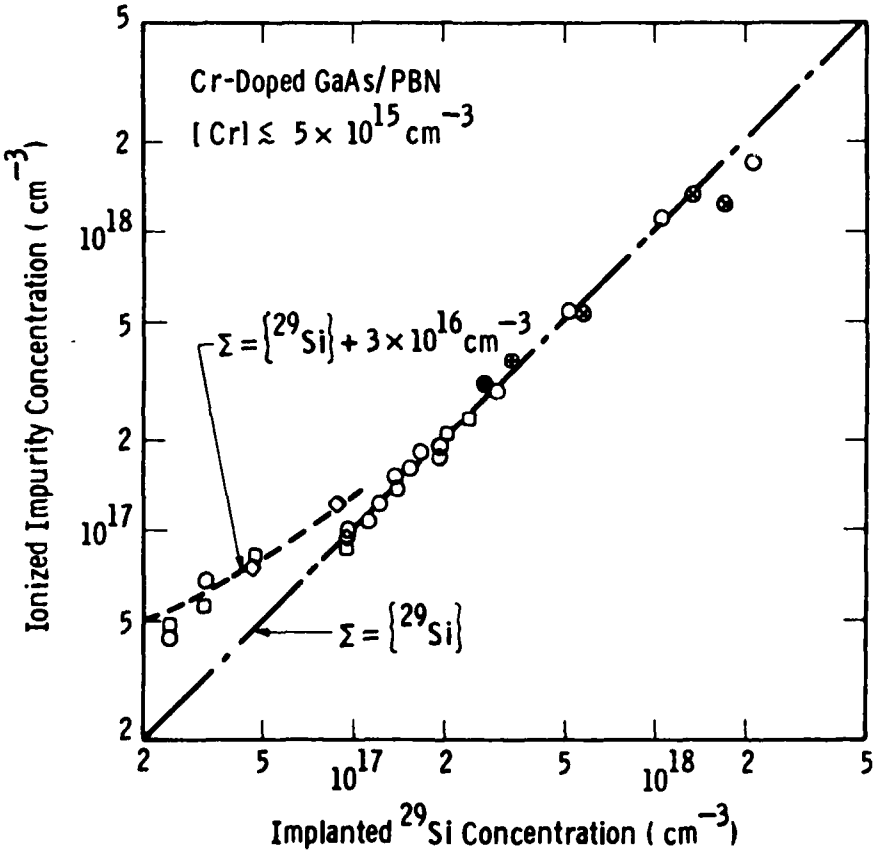

Figure 35 Ionized impurity density as a function of implanted ^{29}Si density for lightly Cr-doped GaAs/PBN. [Cr] ~ 2 x 10^{15} cm^{-3}.

~3 × 10^{16} cm^{-3} additive constant observed for {Si}<9 × 10^{16} cm^{-3} is attributed to 0.5 × 10^{16} cm^{-3} doubly-ionized Cr acceptors plus the ~1 × 10^{16} cm^{-3} centers observed in the undoped material. These Cr centers vanish abruptly at {Si}=9 × 10^{16} cm^{-3} and are not detected in samples implanted to higher concentrations. Detailed evaluation of N_A^- as a function of N_D^+ confirms an abrupt disappearance of 1 × 10^{16} cm^{-3} equivalent singly ionized acceptors at this threshold; there is also some indication that approximately 1 × 10^{16} cm^{-3} donors disappear simultaneously. It can be assumed therefore that Cr doping has no direct effect on the mobility and activation in normal FET layers. There are a number of indirect effects, however. Presence of Cr during the 850°C anneal affects the amphoteric doping ratio of the Si at high net concentrations. Implanted channels are noticeably more abrupt in Cr-doped/PBN material since the Cr tends to behave normally beyond the plane where $\{^{29}Si\}$ drops below 9 × 10^{16} cm^{-3}. Subsequent low-temperature processing (e.g., ohmic contact formation) can lead to reappearance of electrically active Cr. Fig. 36 shows $\Sigma = N_D^+ + N_A^-$, a function of implanted $\{^{29}Si\}$ for Cr-doped (3 to 6 × 10^{16} cm^{-3}) GaAs pulled from fused-SiO_2 crucibles. This $N_D^+ + N_A^-$ again shows complete activation of the implanted Si with saturation of Σ at the 3 × 10^{18} cm^{-3} level becoming unambiguous. The saturation is believed to be common to all three crystal types; only the heavily Cr-doped material was implanted to 5 × 10^{18} cm^{-3} levels. Σ is not well defined at $\{^{29}Si\}$ = 9 × 10^{16} cm^{-3}; at lower Si concentrations the implanted net donor density is not sufficient to overcome the Cr doping and achieve a measurable n-layer. The poorly defined region results from simultaneous formation of a measurable n-layer and neutralization of the Cr which would contribute as much as 2.4 × 10^{17} cm^{-3} to Σ if it all remained active. Disappearance of 5 × 10^{16} cm^{-3} Cr appears to to be accompanied by the disappearance of ~1 × 10^{17} cm^{-3} implanted Si donors. This may be the result of formation of a neutral complex of two Si donors with each Cr atom or a two-step process such as

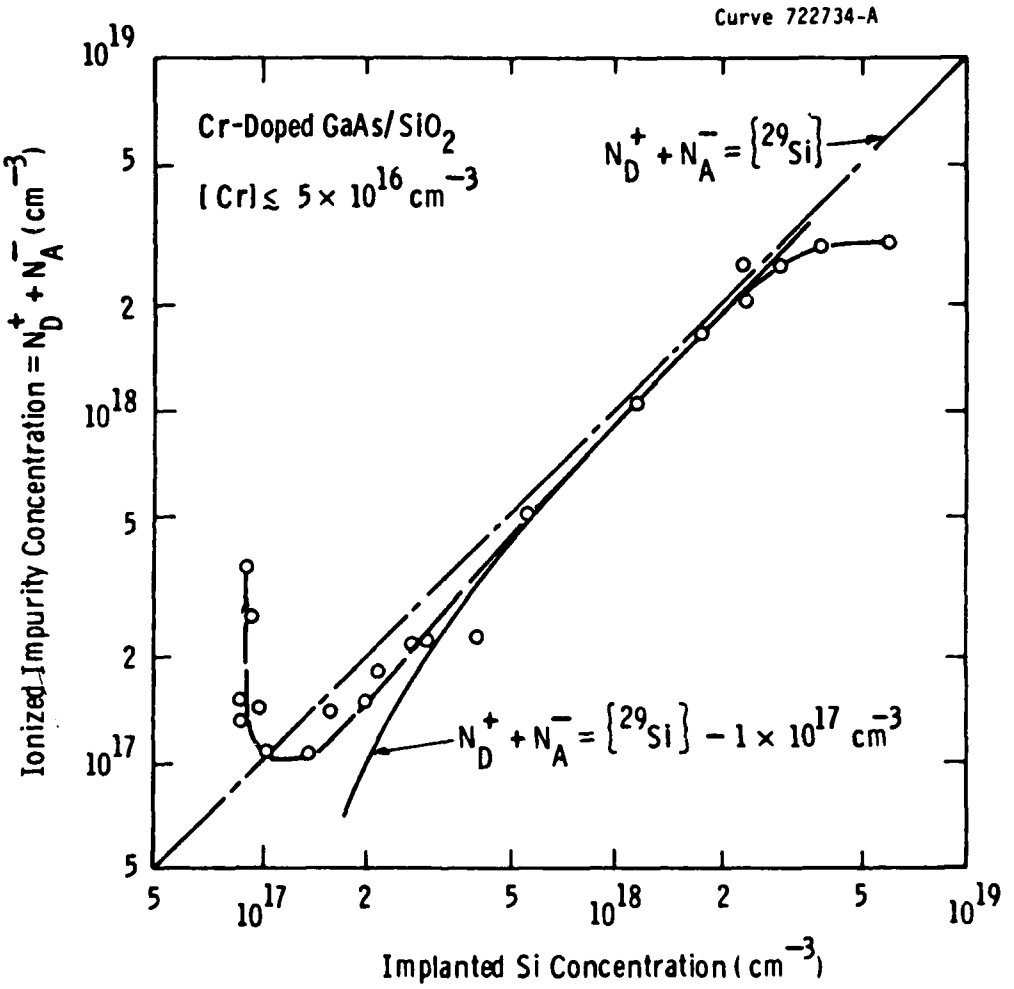

Figure 36 Ionized impurity density as a function of implanted ^{29}Si density for moderately Cr-doped LEC GaAs/SiO_2 [Cr] $\sim 5 \times 10^{16}$ cm^{-3}.

$$\begin{array}{ccccc} Cr^{=} + 2Si^{+} & \rightarrow & (Cr\text{-}Si)^{-} + Si^{+} & \rightarrow & (Si\text{-}Si) + Cr \\ \Sigma = 6 & & \Sigma = 2 & & \Sigma = 0 \end{array} \qquad (10)$$

where the Si donor acceptor is assumed to be stable and the Cr is assumed to outdiffuse.

5.5 Activation and Modeling

Figure 37 summarizes the activation data of the three crystal types discussed previously. This is the result of the same data; mobility is a redundant variable since it is determined by ionized-impurity scattering as is the implanted concentration if the residual impurity and Cr concentrations are known. The three types of crystals are equivalent on this scale for $0.9 \times 10^{17} \leq \Delta \leq 2 \times 10^{17}$ cm^{-3}. Cr doping results in anomalies at lower concentrations and modifies the amphoteric doping ratio at higher concentrations. A more detailed examination employing the differential activation efficiency η_{Δ} to eliminate the effect of residual impurities demonstrates that the activation is substantially affected by Cr doping at all concentrations; this is shown in Fig. 38. The differential activation efficiency of undoped GaAs/PBN crystals begins to drop at $\Delta = 6 \times 10^{16}$ cm^{-3}. Cr doping delays this reduction, but the approximation of constant activation efficiency used to characterize crystals for device fabrication is a fiction made possible by the limited analysis range ($0.9 \times 10^{17} \leq \Delta \leq 1.8 \times 10^{17}$ cm^{-3}).

It appears that the activation efficiency of implanted Si in undoped GaAs/PBN can be described by simple thermodynamic models.[43] Two equations describe the essential physics. First,

$$\{Si^{-}\}/\{Si^{+}\} = K\, n^{2}(T_{a})$$

Curve 729497-A

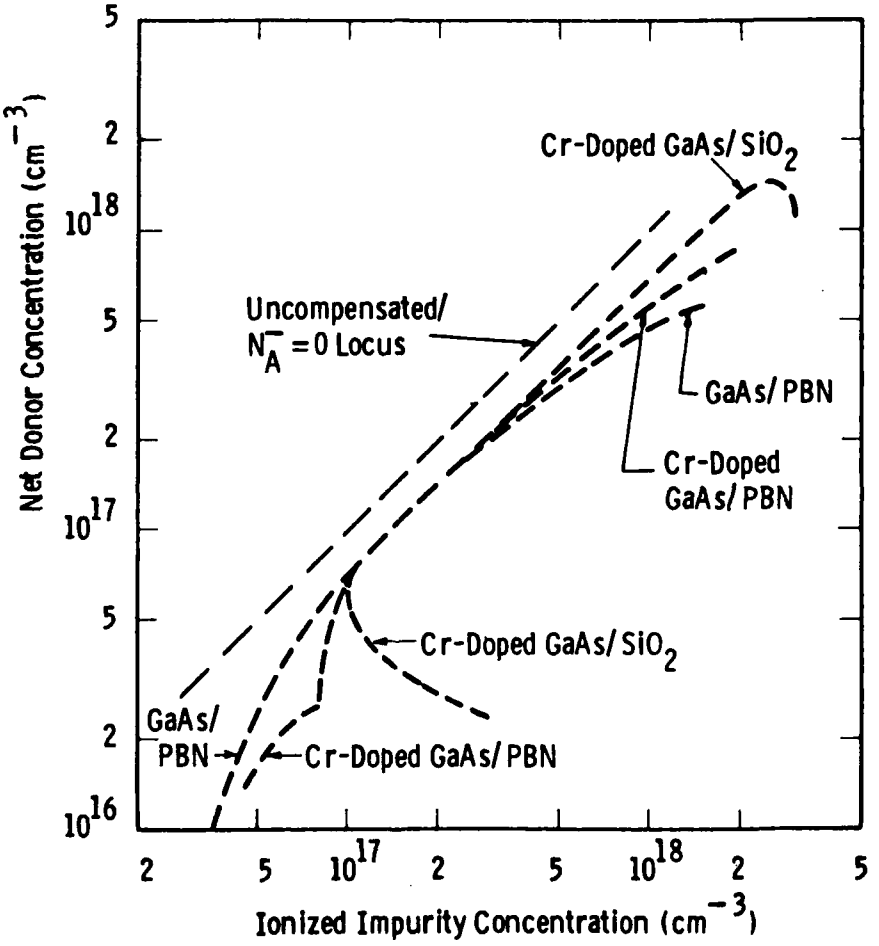

Figure 37 Summary of net donor concentration as a function of ionized impurity concentration for three Cr-doping levels -- $< 5 \times 10^{14}$ cm^{-3}, 2×10^{15} cm^{-3}, 5×10^{16} cm^{-3}.

Curve 729496-A

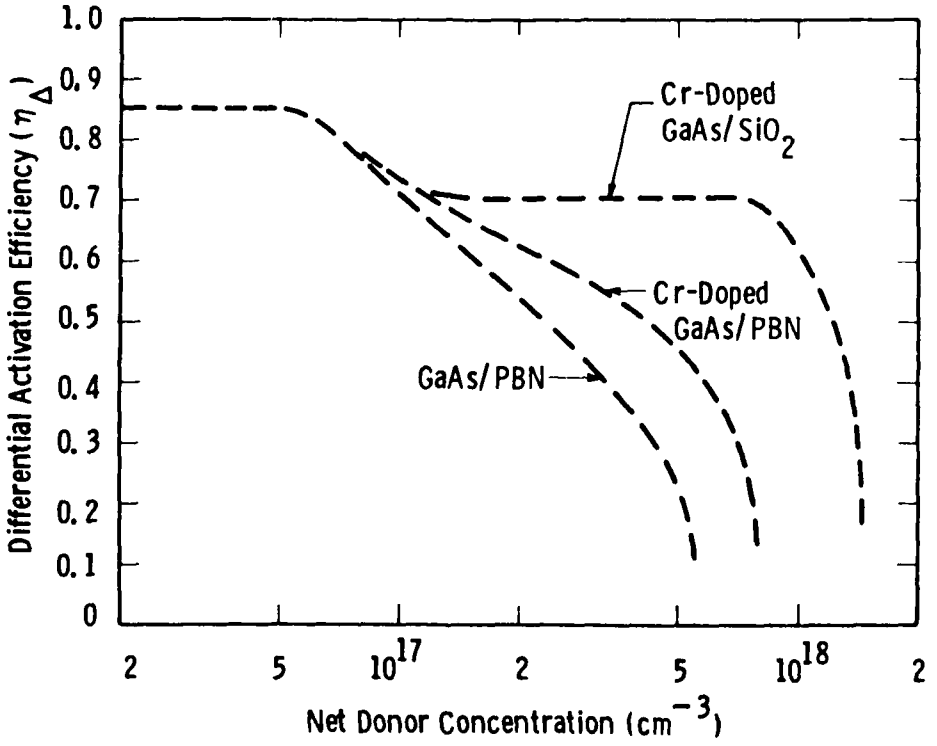

Figure 38 Differential net donor activation efficiency as a function of net donor concentration for three Cr-doping levels -- $< 5 \times 10^{14}$ cm^{-3}, 2×10^{15} cm^{-3}, 5×10^{16} cm^{-3}.

where the Si compensation ratio increases quadratically with the electron concentration at the anneal temperature [$n(T_a)$] and K is a reaction constant which also depends on temperature.

This result is easily derived and should apply to both group IV and group VI dopants; K may be substantially different for group IV and group VI dopants. Second,

$$n(T_a) = \frac{n_i^2(T_a)}{n(T_a)} + K^1 \frac{[V_{As}]}{n(T_a)} + \{Si+\} - \{Si^-\} \qquad (12)$$

where $n_i(T_a)$ is the intrinsic electron density at T_a, and As vacancies are assumed to contribute additional electrons as does the implanted Si. This equation is not specific to Si or group IV n-implants. $n(T_a)$ is determined by the implant at high concentrations so that the compensation ratio varies quadraticly with Δ. The experimental data in undoped GaAs/PBN is in qualitative agreement with this prediction. At lower implant densities, $n(T_a)$ is determined by $[V_{As}]$, and the compensation ratio should be a temperature-dependent constant. Preliminary data suggest $(Si^-)/\{Si^+\} \approx K_o \exp(-.099eV/KT)$ in this dilute limit. Finally, these equations predict that the net concentration marking the transition from dilute to heavy doping should increase with anneal temperature. Anneals at 760°C, 860°C, and 960°C exhibit noticeably non-linear net activation at $\sim 1.0 \times 10^{17}$ cm^{-3}, 2.0×10^{17} cm^{-3}, and 3.5×10^{17} cm^{-3} respectively.

Therefore, it appears possible to describe the electrical behavior of Si implanted into undoped LEC GaAs/PBN without resorting to models which include the effects of residual radiation damage, encapsulant stress, interface gettering, etc. However, the encapsulant plays a key role in the behavior of Cr in Cr-doped material, and the situation is not yet clear.

6. CONCLUSIONS AND FUTURE WORK

During the first year of this research program, significant progress has been made in improving the quality of large-diameter GaAs crystals grown by the high-pressure Melbourn LEC technology and in achieving improved FET channels by direct ion implantation of these substrates. The progress to date is highlighted by the following accomplishments:

A. Crystal Growth

1. Demonstrated reproducible growth of 50- and 75-mm diameter, <100> GaAs crystals free of twin planes and inclusions;

2. demonstrated feasibility of growing larger (100-mm diameter) high-purity, semi-insulating <100> GaAs crystals from 6-kg melts;

3. established that the use of in-situ synthesis, pyrolytic boron nitride crucibles, low water-content B_2O_3 encapsulant, and the gradual increase to the desired crystal diameter are key ingredients to achieving high reproducibility in crystal growth.

B. Substrate Quality

1. Demonstrated that undoped GaAs/PBN and lightly Cr-doped GaAs/PBN crystals consistently yield substrate resistivities approaching 10^8 ohm-cm and higher and are thermally stable under implantation annealing conditions;

2. demonstrated by quantitative SIMS analysis that undoped GaAs/PBN crystals contain the lowest concentrations of shallow donor and acceptor impurities;

3. established by high-impedance Hall measurements that Cr free GaAs/PBN substrates are characterized by 6000 cm^2/vsec mobility, corresponding to total ionized impurity content of 1×10^{16} cm^{-3} range.

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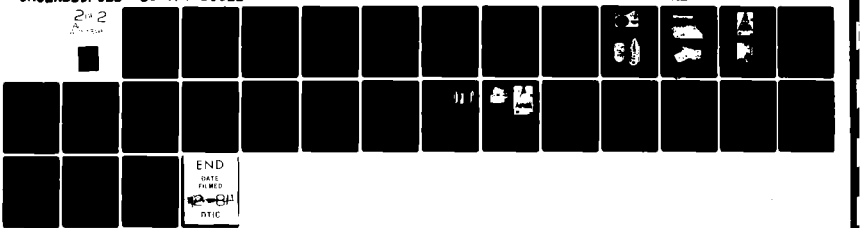

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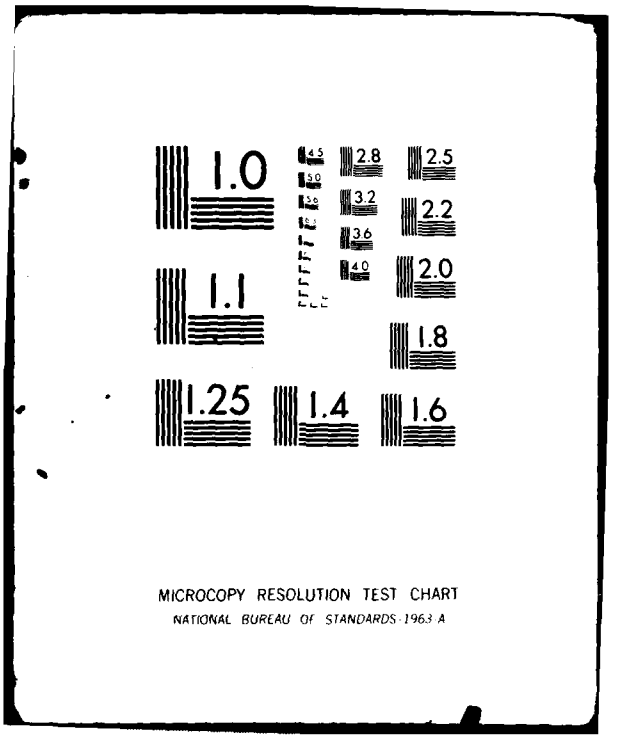
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C. Implantation Of Undoped GaAs/PBN Substrates

1. Demonstrated uniform implant profiles (± 5% from crystal to crystal), high donor activation (~80%) and near theoretical mobilities (4800 to 5000 cm^2/volt sec at peak doping of (1 to 1.3) × 10^{17} cm^{-3} required in power FET channels;

2. achieved channel dopings down to 2 x 10^{16} cm^{-3} and measured mobilities of 5700 at 298K and 14,500 cm^2/vsec at 77K;

3. established that channel mobility is determined solely by ionized impurity scattering and that the substrates are characterized by low 10^{15} donor and 1 × 10^{16} acceptor residual impurities;

4. established a self-consistent model for the observed amphoteric doping behavior and showed that total activation ($N_A + N_D$) is 100%.

Future work will address further various deficiencies in large diameter GaAs crystal growth which the present studies have revealed. These include:

- Need for better diameter control. Twin-free, <100>-oriented LEC GaAs crystals are grown using "manual" diameter control which relies on differential weight signals and operator judgment. This growth method normally results in crystals exhibiting diameter variation $\gtrsim$ 5 mm along the boule length. Experimental large-diameter <100> growth using a diameter-defining "coracle" method have been successfully carried out. These growths demonstrate that diameter uniformities of ±1.0 mm over the entire length of the crystal can be achieved without excessive twinning in the early stages of growth. Future <100> coracle growths will focus on obtaining twin-free material over the full crystal volume.

- Improvements in microscopic crystalline perfection. During the first half of this program, a liquid-encapsulant Czochralski (LEC) technique has been developed for the <100> growth of large-diameter, semi-insulating GaAs crystals free of macroscopic defects, such as twin planes and inclusions, with greater consistency and reproducibility than was possible in the past. Large-diameter (50 to 75mm), <100> LEC GaAs crystals are characterized by radially nonuniform dislocation distributions exhibiting maximum dislocation densities in the mid-10^4 cm^{-2} range. The dislocation distribution is consistent with a thermal-stress generation mechanism arising from sharp thermal gradients associated with the encapsulated melt. Typical axial thermal gradients across the B_2O_3 encapsulating layer in the LEC system are ~140°C/cm. The magnitude of the gradient is

controlled primarily by the B_2O_3 layer thickness and the ambient pressure above the B_2O_3 surface. In the second half of this program, studies will be carried out to reduce the thermal gradients of the system in an effort to reduce dislocation densities below 10^3 cm^{-2} in large diameter LEC GaAs crystals.

- Longitudinal striations have been observed in (100) LEC GaAs crystals for semi-insulating GaAs grown from PBN crucibles and low-resistivity n-type crystals pulled from SiO_2 crucibles. These striations are thought to arise from fluctuations in microscopic growth rate due to thermal asymmetries at the crystal-growth interface. Temperature fluctuations associated with turbulence in large-volume (3kg), encapsulated GaAs melts exhibit temperature excursions of up to 3^oC at the B_2O_3/GaAs interface and 9^oC in the GaAs melt. Future investigations on temperature instabilities in these large-volume encapsulated melts will include the measurement of typical radial temperature gradients and temperature fluctuations as a function of radial position in the LEC system as well as assessing the influence of crucible and seed rotation on striation effects in undoped and Cr-doped GaAs. Residual "frozen-in" stresses can be particularly severe in LEC GaAs crystals and appear to be sensitive to the exact nature of the cool-down program used in bringing the crystal to room temperature after growth. High "frozen-in" stress can lead to severe cracking and wafer fracturing during slicing and subsequent wafer preparation and device fabrication steps. Future studies will assess the influence of thermal annealing on ingot cracking and wafer breakage.

- Understanding the nature of the semi-insulating behavior in undoped GaAs. In the second half of this program investigations will be carried out to establish the exact mechanism which results in the semi-insulating properties reproducibly observed in undoped GaAs crystals pulled from pyrolytic boron nitride crucibles. Studies will specifically address the role of oxygen, boron, and the deep-donor (EL2) level in GaAs/PBN material. Studies will include oxygen doping of GaAs melts as well as oxygen implantation experiments. Effort will be directed toward significantly reducing the boron content of GaAs/PBN material in order to assess the influence of boron on semi-insulating properties of this material. Investigations into the effects of reduced deep-level concentrations on implantation parameters and correlations with device performance will be studied.

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Solid State Electronics Vol. 24, pp. 387–399, 1981
Printed in Great Britain

0038-1101/81/050387-12$02.00/0
Pergamon Press Ltd

GROWTH AND CHARACTERIZATION OF LARGE DIAMETER UNDOPED SEMI-INSULATING GaAs FOR DIRECT ION IMPLANTED FET TECHNOLOGY†

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(*Received* 30 *May* 1980; *in revised form* 25 *August* 1980)

Abstract—The growth of large diameter, semi-insulating GaAs crystals of improved purity by Liquid Encapsulated Czochralski (LEC) pulling from pyrolytic boron nitride (PBN) crucibles and characterization of this material for direct ion implantation technology, is described. Three-inch diameter, (100)-oriented GaAs crystals have been grown in a high pressure Melbourn crystal puller using 3 kg starting charges synthesized *in-situ* from 6/9s purity elemental gallium and arsenic. Undoped and Cr-doped LEC GaAs crystals pulled from PBN crucibles exhibit bulk resistivities in the 10^7 and $10^8\ \Omega$ cm range, respectively. High sensitivity secondary ion mass spectrometry (SIMS) demonstrates that GaAs crystals grown from PBN crucibles contain residual silicon concentrations in the mid 10^{14} cm^{-3} range, compared to concentrations up to the 10^{16} cm^{-3} range for growths in fused silica containers. The residual chromium content in undoped LEC grown GaAs crystals is below the SIMS detection limit for Cr (4×10^{14} cm^{-3}).

The achievement of direct ion implanted channel layers of near-theoretical mobilities is further evidence of the improved purity of undoped, semi-insulating GaAs prepared by LEC/PBN crucible techniques. Direct implant FET channels with $(1–1.5) \times 10^{17}$ cm^{-3} peak donor concentrations exhibit channel mobilities of 4,800–5,000 cm^2/V sec in undoped, semi-insulating GaAs substrates, compared with mobilities ranging from 3,700 to 4,500 cm^2/V sec for various Cr-doped GaAs substrates. The concentration of compensating acceptor impurities in semi-insulating GaAs/PBN substrates is estimated to be 1×10^{16} cm^{-3} or less, and permits the implantation of 2×10^{16} cm^{-3} channels which exhibit mobilities of 5,700 and 12,000 cm^2/Vsec at 298K and 77K, respectively.

Discrete power FET's which exhibit 0.7 watts/mm output and 8 dB associated gain at 8 GHz have been fabricated using these directly implanted semi-insulating GaAs substrates.

NOTATION

- D diffusion coefficient of Si in GaAs
- E_c energy at conduction band edge
- ΔE slope of Arrhenius plot of resistivity
- g Bragg X-ray diffraction vector
- g_m transconductance
- η implant activation efficiency
- n carrier concentration
- N_A ionized acceptor concentration
- N_i implanted silicon concentration
- N_D ionized donor concentration
- R_M projected range of maximum implant concentration
- R_s sheet resistance
- σ_d projected deep standard deviation of implant
- σ_s projected shallow standard deviation of implant
- t time
- T temperature
- μ_H Hall mobility

1. INTRODUCTION

High frequency GaAs MESFETs have received increasing attention over the past decade. Monolithically integrated power and low noise/high gain amplifiers operating at X-band frequencies, as well as high speed GaAs digital logic IC's, are now being developed at several laboratories throughout the world. Fabrication of these monolithic circuits by direct ion implantation of semi-insulating GaAs substrates is highly desirable because of its potential as a reliable, low-cost manufacturing technology. Significant progress is currently being made towards developing a viable planar ion implantation technology, but it is widely recognized that the variable, and often poor quality of semi-insulating substrates is a major limitation at present. GaAs substrates of high resistivity, which retain their semi-insulating properties throughout device fabrication are required, in order to maintain good electrical isolation for low-loss passive circuit elements and low parasitic capacitances associated with active devices. Unfortunately, at the temperatures normally employed in FET processing, the thermal stability of the semi-insulating substrate has often been a severe problem in the past. A common manifestation of the problem is the formation of a conductive surface layer following a thermal annealing process. In ion implantation technology, these anomalous conversion and compensation phenomena which have been observed following post-implantation annealing, adversely affect the implant profile and activation, and can result in poor control of full channel current and pinch-off voltage in directly implanted FET structures. It is probable that the high and variable concentrations of silicon, chromium, oxygen and carbon impurities which are present in typical Cr-doped semi-insulating GaAs substrates contribute to the difficulties in achieving uniform implant profiles, since these impurities can modify their electrical role or redistribute as a result of implantation and thermal annealing. Chromium redistribution has been graphically demonstrated in the case of directly implanted Cr-doped substrates[1]. In addition, typical Cr-doped GaAs substrates contain at least 1×10^{17} cm^{-3} ionized impurities which severely reduce the electron mobility in directly implanted FET channels and degrade the FET performance and frequency limitations. Thermally stable, high resistivity GaAs substrates containing very low concentrations of residual impurities are

†Work supported in part by Office of Naval Research and Defense Advanced Research Agency on Contract No. N00014-80-C-0445.

therefore highly desirable for direct ion implantation device fabrication.

To address the problem of unpredictable properties associated with the semi-insulating GaAs substrates which are available commercially today, a crystal growth facility which utilizes a Melbourn Liquid-Encapsulated Czochralski (LEC) puller† has recently been established at our laboratories. LEC growth was selected over other growth technologies because of its current capability for producing two- and three-inch diameter, (100)- and (111)-crystals of semi-insulating GaAs from which round, large-area substrates can be prepared (Fig. 1). In device processing, handling and processing costs are approximately independent of wafer size, making large-area substrates very attractive for future, low cost manufacturing technology. Perhaps of even more significance is the adaptability of LEC growth to silicon-free, pyrolytic boron nitride (PBN) crucible techniques.[2, 3] offering the potential of semi-insulating GaAs crystals of significantly improved purity, without resorting to intentional Cr doping.

In this paper we report the growth of high purity, two- and three-inch diameter (100)-GaAs crystals pulled from pyrolytic boron nitride crucibles and the characterization of these substrates for direct ion implantation device fabrication. These undoped GaAs/PBN crystals consistently exhibit resistivities approaching $10^8\ \Omega$ cm, are thermally stable under implantation annealing and contain very low total impurity concentrations. The residual silicon and chromium contents are in the mid 10^{14} cm^{-3} range. The improved crystal purity contributes significantly to the high channel mobility (approaching 5,000 cm^2/Vsec at 1×10^{17} cm^{-3} peak donor concentrations of interest for power FET structures) and the uniform, reproducible implant profiles which have been achieved in directly implanted GaAs/PBN substrates. Discrete FETs and monolithic amplifier circuits fabricated on these substrates exhibit excellent transconductances, small signal gains and *rf* output power at X-band frequencies.

2. CRYSTAL GROWTH

Liquid-Encapsulated Czochralski (LEC) growth was first demonstrated experimentally in 1962 by Metz *et al.*[4] for the growth of volatile PbTe crystals, and has since been developed by Mullin *et al.*[5] for several III–V crystals. In this Czochralski technique, the dissociation of the volatile As from the GaAs melt which is contained in a crucible is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a non-reactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure. *In situ* compound synthesis can be carried out from the elemental Ga and As components since the boric oxide melts before significant sublimation starts to take place (~450°C). Compound synthesis occurs rapidly and exothermally at about 820°C under a sufficient inert gas pressure (~60 atm) to prevent sublimation of the arsenic component. Crystal growth is initiated from the stoichiometric melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.

The Melbourn high pressure LEC puller used in this work is a resistance-heated six-inch diameter crucible system capable of charges up to 8–10 Kg weight and can operate at pressures up to 150 atm. The system features a closed-circuit TV for viewing the melt and a differential crystal weight monitor for diameter control.

A number of 2- and 3-inch diameter (100)-GaAs crystals free of major structural defects such as twin planes, inclusions and precipitates have been grown successfully. A photograph of two (100)-GaAs crystals grown using the differential weight signal for diameter control is shown in Fig. 2. Each crystal weighs approximately 3 kg. To achieve reproducible growths of high quality, twin-free crystals, a growth procedure was adopted which included the use of vacuum baking of the boric oxide encapsulant to remove residual moisture—an important factor in maintaining high visibility of the melt-crystal interface during growth, and the gradual increase of the crystal diameter to the desired value during the initial stages of growth (as seen in the crystal displayed on the right-hand side of Fig. 2) to minimize dislocation generation. Semi-insulating GaAs crystals have been prepared from undoped and Cr-doped melts synthesized *in-situ* from high purity elemental arsenic and gallium charges and contained in both fused silica and pyrolytic boron nitride crucibles. Selected semi-insulating GaAs crystals have been sawn and polished to provide substrates for device fabrication. Selection of both Cr-doped and undoped crystals was based on structural, chemical and electrical characterizations which are described below.

3. SUBSTRATE QUALITY

3.1 *Crystalline perfection*

It has been shown on an experimental basis that crucible-pulled GaAs crystals can be grown free of dislocations at small crystal diameters, usually ≤0.5 in and crystal lengths <3 in[6]. For these small crystals, successful dislocation-free growth depends upon the following growth conditions: (i) a Dash-type seeding method in which the seed is grown with a thin neck before increasing the diameter to form the crystal cone[7]; (ii) a melt which is close to stoichiometry and a small axial temperature gradient at the interface[8]; (iii) the growth interface maintained flat to convex toward the melt[9]. In addition, the angle of the crystal cone is also important for dislocation-free growth. If the cone angle is too large, dislocation generation can result from the high internal stresses which develop as the crystal cone emerges from the B_2O_3 encapsulant[10].

Although large diameter (≤3 in) LEC GaAs crystals grown in the ⟨100⟩ axial orientation are free of gross structural imperfections, such as twins and inclusions, these crystals are usually characterized by high background densities of dislocations (10^4–10^5 cm^{-2}), such as shown by the X-ray reflection topograph of Fig. 3 for a typical (100) LEC GaAs wafer. Our preliminary investigations on improving the structural quality of large

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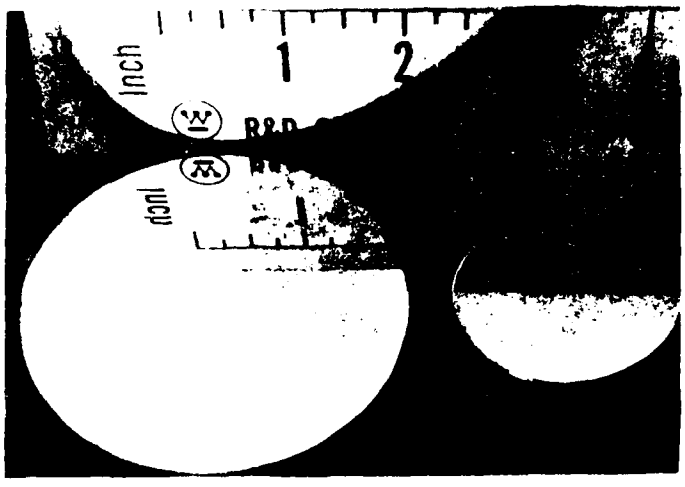

Fig. 1. Round two- and three-inch diameter GaAs wafers cut from ⟨100⟩-axially oriented crystals pulled in a Melbourn Liquid Encapsulated Czochralski puller.

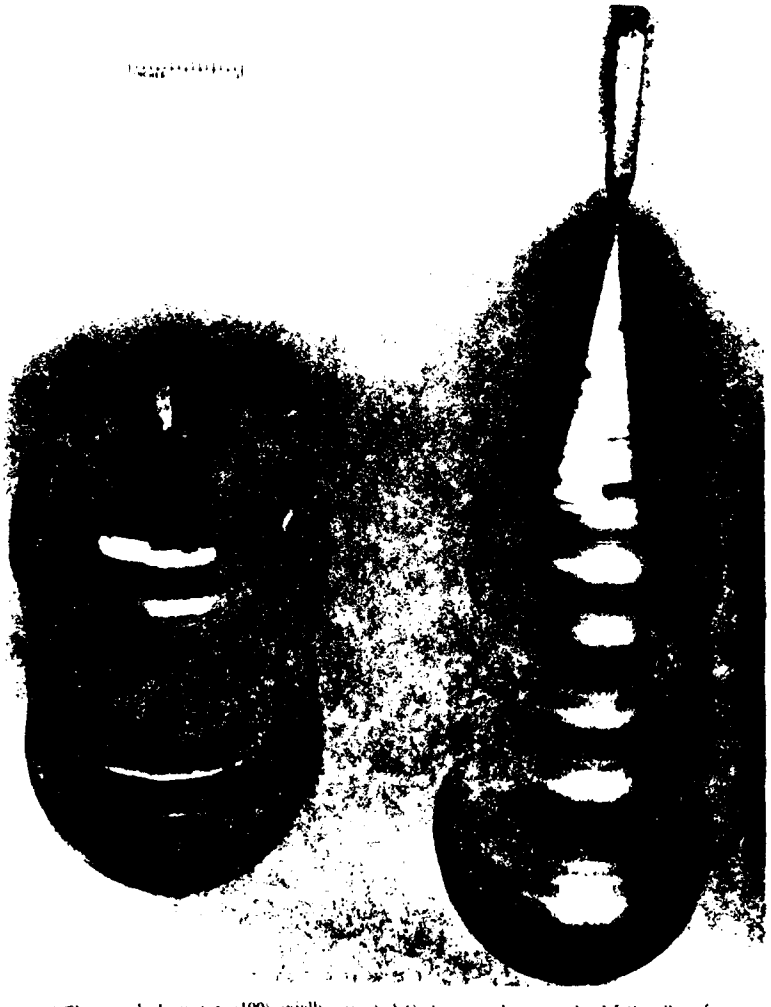

Fig. 2. Two- and Three-inch diameter, ⟨100⟩-axially oriented GaAs crystals grown by LEC pulling from six-inch diameter pyrolytic boron nitride crucibles.

Fig. 3. Reflection X-ray topograph ($g = (315)$) of LEC grown GaAs substrate pulled from boron nitride crucible Area = 1.84 cm^2.

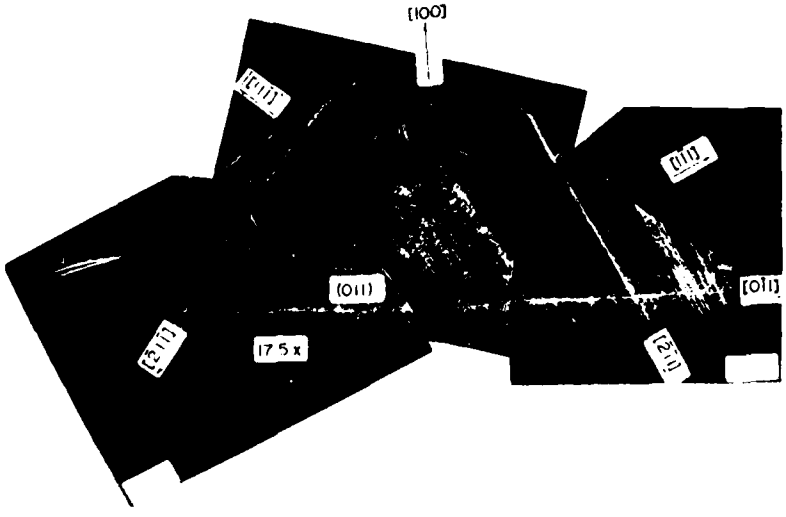

Fig. 4(a). Reflection X-ray topograph ($g = (315)$) of (011) longitudinal section for a shallow cone angle. Crystal pulled from pyrolytic boron nitride crucible.

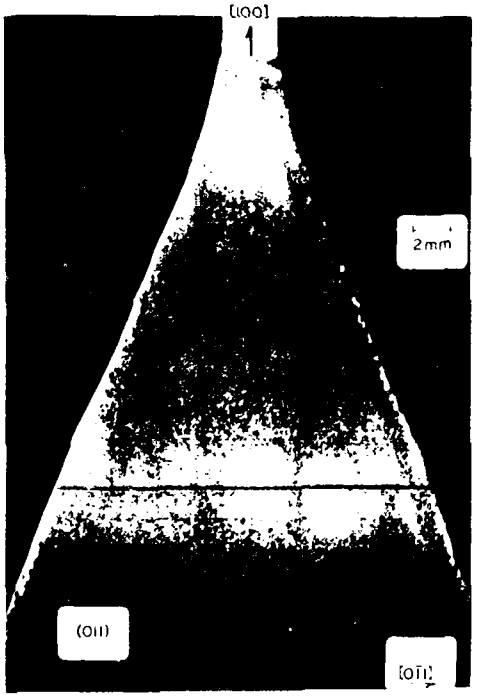

Fig. 4(b) Reflection X-ray topograph (g = (260)) of (011) longitudinal section for cone angle of 27°. Crystal pulled from pyrolytic boron nitride crucible.

Fig. 15. Centerless ground GaAs boule with (110) orientation flat. Polished slices are 1.975 ± 0.001 in. dia. and 0.018 in. thick.

Table 1. High sensitivity secondary ion mass spectroscopy analysis† of LEC semi-insulating GaAs crystals pulled from high purity pyrolytic boron nitride crucibles.

Crystal	C	O	Si	S	Se	Te	Cr	Mg	Mn	B	Doped Yes	Doped No
BN-1 (s)	2 e 15	L 5 e 16	4.8 e 14	5.7 e 14	2 e 13	1 e 12	3.6 e 14	1 e 15	7 e 14	2.3 e 15		✓
BN-2 (s)	1 e 16	6 e 16	6 e 14	2 e 15	1 e 15	7 e 13	5.6 e 14	4 e 14	8 e 14	L 7 e 17		✓
BN-3 (s)	3 e 15	L 3 e 16	9.3 e 14	4.2 e 14	3 e 14	3 e 12	4.3 e 14	2 e 15	1 e 15	5.4 e 17		✓
BN-4 (s)	-	-	2 e 15	8 e 14	2 e 14	1 e 14	1 e 16	2.5 e 15	2 e 15	L 5 e 17	✓ Cr	
BN-6 (t)	2.9 e 15	9.8 e 15	5.4 e 14	5 e 14	9.4 e 13	1 e 12	5.4 e 14	2.5 e 15	L 7 e 15	6.9 e 17		✓
BN-8 (s)	L 1 e 16	3.7 e 16	8.7 e 15	L 1 e 15	5 e 13	7 e 12	2.2 e 14	8.5 e 14	5.3 e 14	7.3 e 16	✓ Si	
BN-10 (s)	2 e 15	1 e 16	8.6 e 14	L 5 e 15	7 e 14	7 e 12	3.7 e 14	3.6 e 15	L 2 e 15	2 e 18		✓
BN-11A (s)	4.3 e 15	L 8 e 16	6.4 e 14	1 e 15	8 e 13	6 e 12	6.4 e 15	3.2 e 15	L 4 e 15	L 9 e 17	✓ Cr	
BN-11B (s)	3 e 15	L 3 e 16	7.6 e 14	8.7 e 14	1 e 14	8 e 12	6.3 e 15	4.4 e 15	L 6 e 15	L 9 e 17	✓ Cr	
BN-12 (s)	2 e 16	7 e 16	1 e 15	2 e 15	5 e 14	6 e 13	3.2 e 15	3 e 14	8 e 14	L 8 e 17	✓ Cr	
Detection Limit	-	-	3 e 14	3 e 14	5 e 12	5 e 12	4 e 14	3 e 14	7 e 14	8 e 13		

†SIMS analysis courtesy Charles Evans & Associates, San Mateo CA

diameter GaAs crystals have concentrated on determining the optimum conditions for initiating dislocation-free growth. Figures 4(a) and (b) show X-ray reflection topographs of longitudinal sections of seed-end cones for two (100) GaAs crystals corresponding to two different cone angles: (a) a relatively shallow cone and (b) a steeper cone of 27° to the crystal axis. In both cases dislocation-free growth is initiated using a Dash-type seeding. As the cone diameters increase, the dislocation densities increase, particularly in the crystal interior, together with activation of glide planes; however, the rate of dislocation multiplication has been reduced by the steeper cone angle (Fig. 4(b)).

3.2 *Impurity content*

Secondary ion mass spectrometry bulk analysis† of LEC GaAs material pulled from both quartz and pyrolytic boron nitride crucibles at our laboratories, as well as large-area boat-grown substrates purchased from an outside supplier have been carried out. A wide range of impurity species were examined and the data clearly show that the lowest concentrations of electrically active impurities are achieved in LEC growths from PBN crucibles. The detailed SIMS data for crystals pulled from pyrolytic boron nitride crucibles are shown in Table 1. Quantitative estimates of impurity concentrations were obtained by calibration against GaAs samples which had been ion implanted with known does of specific impurities. The comparative results are shown in Fig. 5 where the markers on each bar represent data for different crystals. Residual silicon concentrations in the mid 10^{14} are observed in GaAs/PBN samples compared to levels which range up to 10^{16} cm^{-3} in crystals grown in quartz containers. The residual chromium content in undoped LEC GaAs crystals pulled from either PBN or fused silica crucibles is below the detection limit of the SIMS instrument, estimated to be

†The SIMS analyses were performed at Charles Evans and Associates, San Mateo, CA using a Cameca IMS-3F ion microanalyzer.

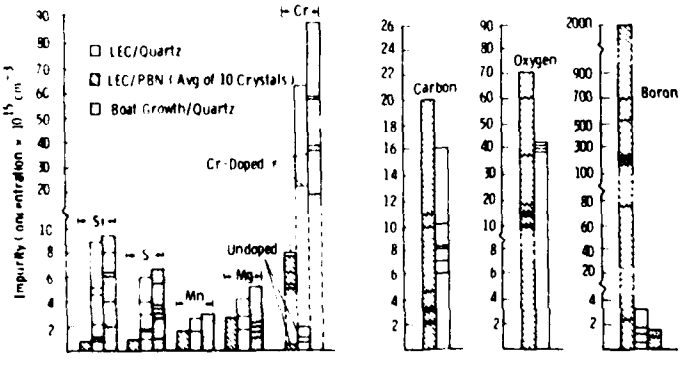

Fig. 5. Bulk SIMS analysis of semi-insulating GaAs prepared by LEC and horizontal Bridgeman growth. Horizontal makers indicate different crystal samples.

in the low 10^{14} cm^{-3} range. Analyses of LEC-grown crystals pulled from Cr-doped melts contained in quartz crucibles reveal that the Cr content (typically 2×10^{16} cm^{-3} at the seed-end and approaching 10^{17} cm^{-3} at the tang) is close to the anticipated doing level based on the amount of Cr dopant added to the melt and its reported segregation behavior[11]. Cr dopant levels of (2 to 8) $\times 10^{16}$ cm^{-3} were observed in the boat-grown samples. The reduced concentration of shallow donor impurities in growths from PBN crucibles permits lower Cr doping levels to be utilized, as shown in Fig. 5 where typical Cr dopant concentrations range from 3×10^{15} cm^{-3} at the seed end to 8×10^{15} cm^{-3} at the crystal tang end.

Additional SIMS studies indicate that LEC growths from PBN crucibles generally result in high boron concentrations (10^{17} cm^{-3} range) in the GaAs material versus low 10^{15} cm^{-3} concentrations in quartz crucible growth. No significant differences in carbon ($\sim 10^{16}$ cm^{-3}) oxygen (10^{16} cm^{-3}), selenium (mid 10^{14} cm^{-3}) and tellurium ($<10^{14}$ cm^{-3}) contents of different GaAs samples are revealed by these investigations. Iron concentrations are estimated to be below 10^{15} cm^{-3} in all samples. The results reported in Section 4 suggest that boron in GaAs/PBN substrates remains electrically neutral through implantation processing and does not contribute significantly to ionized impurity scattering.

3.3 *Electrical characterization*

Resistivity and thermal stability measurements were carried out on LEC-grown GaAs substrates to determine the suitability of the substrates for ion implantation studies. Additional assessment of the substrate quality was provided by measurements of the transport properties of *n*-doped layers formed by direct ion implantation into the substrate.

The axial resistivity variation along undoped and Cr-doped GaAs crystals is shown in Fig. 6. Substrate resistivities in the 10^{8}–$10^{9}\,\Omega$ cm range are observed in Cr-doped substrates (containing high 10^{16} cm^{-3} Cr concentrations) compared to resistivities of 10^{7}–$10^{8}\,\Omega$ cm in undoped GaAs/PBN substrates. Lightly Cr-doped GaAs/PBN crystals (mid 10^{15} cm^{-3} Cr content) exhibit resistivities greater than $3 \times 10^{8}\,\Omega$ cm. Undoped GaAs crystals pulled from fused silica crucibles show lower resistivities and a greater variation along the crystal. Variable results were obtained from crystal to crystal, varying from 10^{6} to $10^{7}\,\Omega$ cm in one to resistivities in the $10^{3}\,\Omega$ cm range in another crystal.

The mechanism of electrical compensation in semi-insulating GaAs has been studied extensively[12, 13] and it has been tacitly accepted that semi-insulating behavior in undoped GaAs results from oxygen compensation—an impurity which is introduced, usually in the form of Ga_2O_3 or As_2O_3, to suppress silicon contamination from dissociation of the SiO_2 ampoule in horizontal Bridgeman/gradient freeze growths[14]. In LEC-grown crystals oxygen is unintentionally incorporated; however, its role in determining the electrical properties is not understood at present. In Cr-doped GaAs, high resistivity is believed to result from the compensation of shallow donors by the deep chromium acceptors. Zucca[13] has proposed a model which includes both a deep acceptor (Cr) and deep donor (oxygen) to interpret experimental resistivity data in lightly Cr doped GaAs (5×10^{15} cm^{-3} Cr). The assignment of oxygen to the measured deep donor level at about 0.64–0.72 eV from the conduction band edge is, however, controversial[15]. Zucca's data indicate predominantly hole conduction from chromium acceptors ($Ec - 0.83$ eV) in highly Cr-doped substrates (6×10^{16} cm^{-3} Cr).

Plots of log resistivity versus reciprocal temperature for undoped and Cr doped LEC GaAs crystals pulled from pyrolytic boron nitride and fused silica crucibles are shown in Fig. 7. All the samples measured showed conduction by electrons to be dominant and independent of the Cr content between 2×10^{15} and 8×10^{16} cm^{-3}. An activation energy of 0.76 eV was measured for all sample

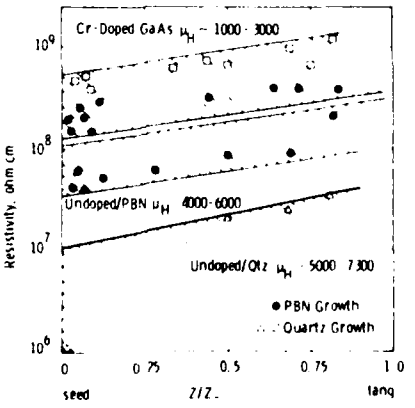

Fig. 6. Axial resistivity variation along LEC grown GaAs crystals pulled from quartz and pyrolytic boron nitride crucibles

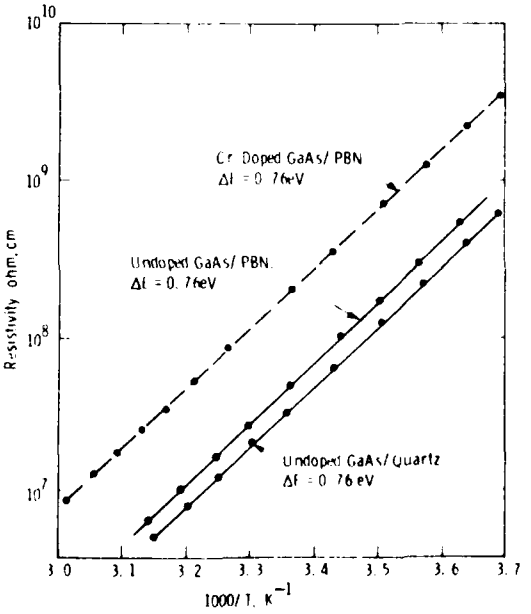

Fig. 7. Log resistivity as function of reciprocal temperature for LEC GaAs grown in PBN and quartz crucibles.

types. While these results confirm the importance of the deep donor level in semi-insulating GaAs, no other conclusions can be drawn at present and further studies are in progress.

Although direct evaluation of the carrier mobilities and net donor and acceptor concentrations in semi-insulating GaAs substrates is made difficult by the high sample impedance and the complexity of data interpretation[16], high impedance Hall measurements performed at ambient temperature indicate high apparent electron mobilities of between 4000 and 7,200 cm^2/Vsec in undoped GaAs pulled from quartz or PBN crucibles and is a qualitative indication of the high purity of these samples. In contrast, the measured electron mobilities in all semi-insulating Cr-doped samples are in the 1,000–3,000 cm^2/Vsec range.

Thermal stability of substrates for ion implantation was assessed by means of resistivity measurements following an encapsulated anneal of the semi-insulating slice (prior to implantation) to determine whether any conducting surface layers formed as a result of thermal treatment. Samples for the unimplanted, encapsulated anneal test were prepared using the same process as is used for implantation. The wafers were prepared by etching to remove cutting damage and bromine-methanol polishing on the front surface to 0.020 in thickness. A 900 Å layer of Si_3N_4 was deposited on the front surface by a plasma-enhanced silane-nitrogen reaction. These depositions were performed in a modified LFE PND301 reactor at a substrate temperature of 340°C, nominal gas flows of 40 sccm 1.5% SiH_4 in Ar and 3 sccm N_2, and 100 W rf power, which yielded 75 Å/min deposition rates. A 2500 Å thick layer of 7% phosphosilicate glass (PSG) was also deposited at 420°C on both surfaces prior to annealing as protection against pinholes in the nitride encapsulant (and is also utilized for pattern definition with selective implants in FET processing). The wafers were annealed at 860°C for 15 min in a forming gas atmosphere. Surface sheet resistances exceeding 10^6 Ω/□ are desired after annealing to ensure isolation of passive as well as active elements in analog IC processing.

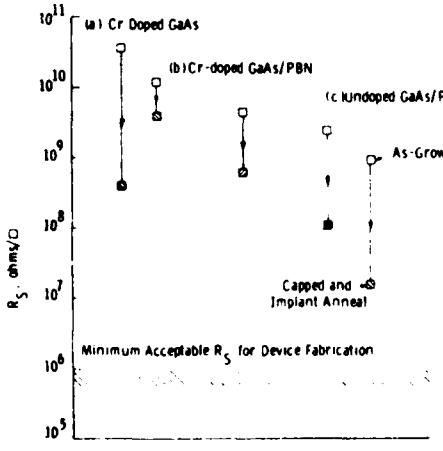

Fig. 8. Thermal stability of undoped and Cr-doped LEC GaAs substrates after Si_3N_4 capping and 860°C/15 m annealing.

Typical sheet resistance data for semi-insulating undoped and lightly Cr-doped GaAs/PBN substrates and conventionally Cr-doped GaAs substrates before and after encapsulated anneals are shown in Fig. 8. Some degradation in the sheet resistance was always observed as a result of the thermal treatment, but the leakage currents measured in these low field measurements (10^3 V/cm) and the rf losses observed in monolithic circuits fabricated on these substrates were low. In particular, surface leakages of $>30\ \mu$A at 15 V bias and high breakdown voltages of 25 V were measured in interdigitated capacitor structures (5 μm separation and 13.2 mm periphery) to test the performance under the high operating fields normally utilized in monolithic circuits.

ION IMPLANTATION

Direct ion implantation of undoped and Cr-doped GaAs substrates was performed at ambient temperature using ^{29}Si ions in a 400 keV Varian/Extrion ion implanter. The Si beam was generated from a SiF_4 source so that the Si isotope ratios could be measured and $^{29}Si^+$ beam purity assured. The implants discussed here were performed through a 900 Å thick front surface Si_3N_4 encapsulation. Separate sequences of bare implants indicate that the activation efficiency and mobility data are identical in both cases. High sensitivity SIMS profiles of ^{29}Si and ^{52}Cr after a 4×10^{12} cm^{-2}–350 keV $^{29}Si^+$ implant through Si_3N_4 are shown in Fig. 9; these specimens received the standard PSG overlay and 860°C/15 min anneal. In Fig. 9, the surface ^{29}Si and ^{28}Si peaks are probably the result of matrix effects in the SIMS measurements and recoil implantation from the Si_3N_4 layer. The effects of recoil implantation are not detected in electrical measurements because of surface depletion phenomena. Surface accumulation of Cr in both Cr-

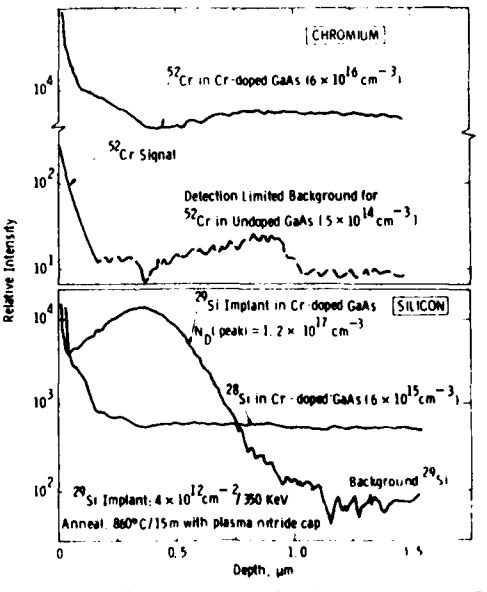

Fig. 9. SIMS profiles of silicon and chromium distributions in Cr doped GaAs after ^{29}Si implant and annealing. Residual Cr profile of implanted GaAs/PBN sample is also shown.

doped and undoped LEC GaAs substrates is typical of published results[1]. In contrast to these published data, only slight Cr depletion is observed near the peak of the $^{29}Si^{+}$ implant.

Electrical profiles of ^{29}Si implants in semi-insulating GaAs were obtained by C–V measurements using evaporated Al Schottky barrier diodes. Plots of the variation of net donor concentration with depth of implant in undoped GaAs/PBN substrates are shown in Fig. 10 and represent the uniformity across each slice and from slice-to-slice in this material in both activation efficiency and profile shape. The data shown was measured on three slices cut from the first half of an undoped GaAs/PBN crystal. The data show a high degree of uniformity for direct substrate implants and similar uniformity and reproducibility has been achieved for implant energies between 125 and 400 keV. As shown in Fig. 10, the measured profiles can be fitted to the tabulated joined half gaussian profile[17], provided modifications† are made to the latter to allow for energy loss in the Si_3N_4 and diffusion. The depth of maximum concentration (R_M) is 2650 Å and the deep and shallow standard deviations (σ_d and σ_s) are 1000 and 1400 Å respectively.

The profiles shown in Fig. 11 are typical of ^{29}Si implants into Cr-doped GaAs substrates. Poor agreement with the theoretical LSS profile is apparent, although SIMS profiling of the ^{29}Si implants in Cr-doped substrates yields approximately gaussian distributions (see Fig. 9). The abrupt fall-off of the electrical profiles near the $R_m + \sigma_d$ depth suggests either Cr accumulation in the region and/or Cr depletion at shallower depths. Achievement of this profile is sensitive to the energy of the channel implant and the dose of any shallow (125 kV) implant employed to increase the electron concentration at the surface. Implantation of ^{29}Si into Cr-doped GaAs has generally been characterized by poorer uniformity of activation and profile shape compared to undoped substrates, particularly in highly Cr-doped substrates which exhibit unpredictable and often anomalous implant profiles.

More detailed measurements of the electrical activation of ^{29}Si implants in semi-insulating GaAs/PBN substrates are shown in Fig. 12. Implantations through the Si_3N_4 encapsulant layer at 100, 200 and 400 keV energies were utilized to obtain uniform profiles in this series of experiments. The net donor concentration was obtained directly from C–V measurements and the implanted concentration from the measurement dose and the

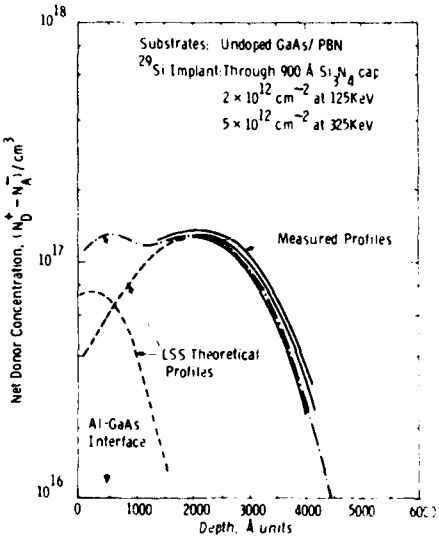

Fig. 10. Uniformity of implant profiles in undoped GaAs/PBN substrates measured by C–V profiling. Implants performed through 900 Å thick Si_3N_4 layer.

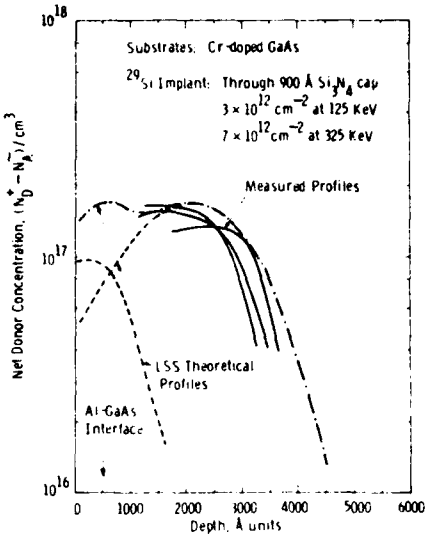

Fig. 11. Implant profiles in Cr-doped GaAs substrates measured by C–V profiling. Implants performed through 900 Å thick Si_3N_4 layer.

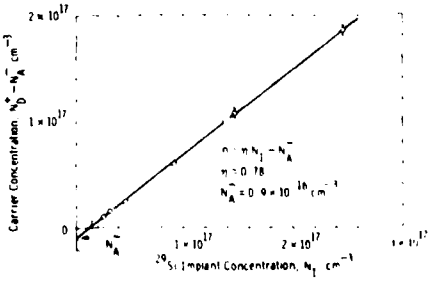

Fig. 12. Activation efficiency (η) and substrate acceptor concentration (N_A^-) for ^{29}Si implants in undoped GaAs/PBN substrates

†The modifications include the assumption that the stopping power of the Si_3N_4 layer is approximately the same as GaAs; the inclusion of third moment estimates in calculating the R_m from tabulated values and the allowance for diffusion broadening according to

$$\sigma^2 = \sigma^2 + 2Dt$$

where

$2Dt \simeq 3 \times 10^{-11}$ cm^2, with $D = 1.5 \times 10^{-14}$ cm^2/sec.

channel thickness as calculated from the profile data and assumed to be $R_m + \sqrt{(\pi/2)}\,\sigma_d$. Corrections for surface depletion assuming a 0.6 eV surface barrier and a 40% deposition of the low energy implant in the nitride layer were made. Figure 12 indicates an activation efficiency of 78%. Similar measurements of other GaAs/PBN substrates indicate that the activation efficiency increases with increasing chromium content (70–80%/undoped; 75–85%/low Cr (8×10^{15} cm^{-3}); 85–100%/high Cr (6×10^{16} cm^{-3}). The somewhat lower net activation efficiencies observed in implanted undoped and lightly Cr-doped GaAs/PBN substrates are believed to reflect both the amphoteric nature of Si in GaAs and a shift in the defect equilibria on the As sublattice with Cr doping. Preliminary results suggest that failure to achieve 100% donor activation of the implanted Si is related to compensation of Si_{Ga}^{+} by both Si_{Ga}–V_{Ga} and Si_{As} centers, and that the Si_{As} concentration is systematically reduced by increasing the Cr concentration.

Figure 12 also indicates the existence of a small threshold dose for the onset of electron conduction in the implanted channel. This threshold corresponds to the density of levels which must be populated to raise the Fermi level to near the conduction band edge. Presumably, this threshold donor concentration is required to repopulate deep donors which were initially ionized by residual acceptor impurities in the undoped GaAs/PBN material. A threshold concentration of 0.9×10^{16} cm^{-3} is determined for the intercept in Fig. 12, and corresponds to the residual ionized acceptor density N_A in the substrate. In contrast, implants into GaAs substrates having high Cr dopant indicate a required threshold concentration in the $(5\text{–}10)\times10^{16}$ cm^{-3} range, increasing from seed-end substrates to tang-end substrates in these Cr-doped crystals. These results suggest that high Cr concentrations in GaAs/PBN substrates serve no useful purpose and contribute to excessive ionized impurity scattering, compensation and redistribution phenomena.

Low-field Hall effect mobilities as a function of the peak donor concentration have been measured in directly implanted channels in undoped and Cr-doped GaAs substrates and are shown in Fig. 13. Data from two undoped GaAs/PBN and three conventional Cr-doped GaAs crystals grown by the LEC technique, as well as Cr-doped boat-grown GaAs, are shown. The implants were performed at energies between 250 and 400 keV, with nitride caps and with single and dual energy implants. ^{29}Si implants into semi-insulating GaAs/PBN substrates show the highest mobilities: at peak donor concentrations of about 1×10^{17} cm^{-3}, mobilities of 4,800–5,100 cm^2/Vsec are measured compared with mobilities in 3,700–4,500 cm^2/Vsec range for Cr-doped substrates prepared by LEC or boat growth. In lightly doped channel layers (2×10^{16} cm^{-3}) the observed differences are considerably larger—an electron mobility of 5,600 cm^2/Vsec in undoped GaAs/PBN substrates vs 3,000 cm^2/Vsec in Cr-doped substrates. The measured mobilities of directly implanted channel layers in GaAs/PBN correspond to a mobility averaged over the implanted ^{29}Si conductivity profile. Since over the range of donor concentrations investigated, the theoretical mobility is a slowly varying

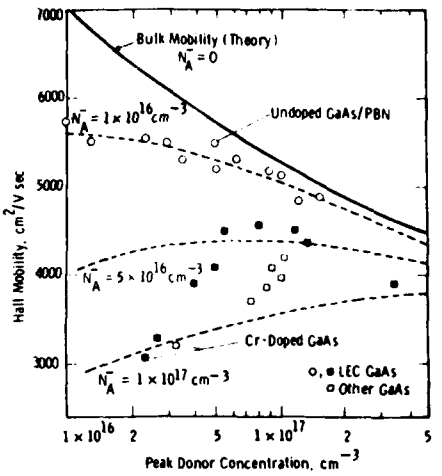

Fig. 13. Measured direct ^{29}Si implant mobility in semi-insulating undoped and Cr doped GaAs compared with theoretical bulk mobility.

function of the net donor concentration for uniform, bulk material[18], the averaged mobility of the implanted layers can be reasonably compared to that given by theory as shown by the dashed lines of Fig. 13. The higher mobilities observed in undoped GaAs/PBN substrates are consistent with a compensating acceptor density of about 1×10^{16} cm^{-3}, in agreement with the value derived from observations of the threshold dose for the onset of electrical activity (Fig. 12).

Mobility measurements were also performed at 77K for the implanted layers in semi-insulating GaAs/PBN substrates. A plot of mobility as a function of peak donor concentration at 77 and 298K is shown in Fig. 14. The 77K mobility of 12,000 cm^2/Vsec which has been achieved in lightly doped channels (2×10^{16} cm^{-3}) is to our knowledge the highest mobility which has been achieved by direct ion implantation into semi-insulating substrates and is comparable to the mobilities which have been attained in epitaxially grown layers (see, for example, the data compiled by Rosztoczy and Kinoshita[19].

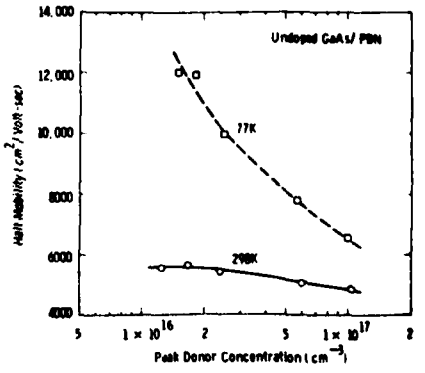

Fig. 14. Measured mobility at 77 and 298K in directly implanted undoped GaAs/PBN substrates.

5. DISCUSSION AND SUMMARY

The progress made towards developing higher purity, high resistivity GaAs crystals through the use of LEC pulling from pyrolytic boron nitride crucibles is reported in this paper. The intent is to achieve stable, semi-insulating substrate properties without resorting to intentional doping with chromium (or at least, to reduce the Cr dopant content of GaAs significantly) in order to avoid the serious redistribution problems associated with this impurity at quite low temperatures and their potentially harmful effects on FET device performance and reliability.

It has been shown that large diameter GaAs crystals grown from high purity melts in PBN crucibles contain significantly lower concentrations of electrically active residual impurities than LEC and boat-grown crystals prepared in fused silica containers. In particular, residual silicon concentrations of mid 10^{14} cm^{-3} were determined by quantitative SIMS analyses compared to silicon contents of up to 1×10^{16} cm^{-3} in other GaAs crystals. High boron and carbon concentrations were, however, observed in GaAs/PBN crystals, but these impurities do not appear to affect the electrical transport properties of ion implanted layers formed in these substrates. Semi-insulating behavior is achieved in undoped GaAs/PBN substrates, although the concentrations of deep acceptor impurities, such as Cr and Fe, are at least an order of magnitude less than the Cr doping levels normally encountered in conventional semi-insulating GaAs. The as-grown resistivity and sheet resistance of thermally annealed undoped GaAs/PBN substrates fall in the mid to high $10^7\,\Omega$ cm and $10^7\,\Omega/\square$ ranges, respectively. Although these resistivities are lower than those of conventional Cr-doped GaAs, acceptably low leakages and rf losses are attained in FETs and analog circuits fabricated on this material. Light Cr doping (low 10^{15} cm^{-3}) enables higher resistivities to be attained without adversely affecting the measured electron mobilities in implanted layers.

Direct ion implantation studies of undoped GaAs/PBN substrates using ^{29}Si implants yield highly reproducible implant profiles showing excellent agreement with LSS theoretical predictions. The results suggest a weakly amphoteric behaviour of the silicon implants in undoped or lightly Cr-doped GaAs/PBN substrates and demonstrate an excess compensating acceptor concentration of about 1×10^{16} cm^{-3} in these substrates. High channel mobilities of 4,800–5,000 cm^2/Vsec are obtained in directly implanted channels with $(1\text{–}1.5) \times 10^{17}$ cm^{-3} peak donor concentrations required for X-band power FET structures.

Excellent power FET performance has been demonstrated from 1 μm gate length devices fabricated on semi-insulating GaAs/PBN substrates in our laboratories[20]. Directly implanted devices exhibit g_m values of about 100 mmhos/mm, small signal gains at 8 GHz of over 11 dB and an rf output power of 0.75 W/mm. A total output power in excess of 1 W with 5 dB gain at 8 GHz was measured recently from a directly implanted FET device (2,400 μm gate). Preliminary evaluations also indicate that device characteristics of improved uniformity are attained on semi-insulating GaAs/PBN substrates—a significant factor for the design of circuit parameters in monolithic integrated GaAs circuits.

GaAs device fabrication has traditionally been carried out on irregularly-shaped substrates because of the lack of uniformly round substrates in the past. The coracle diameter control† is a step in this direction, but is available only for (111) growths and from our limited experience of this method is found to adversely affect the purity and structural quality of LEC crystals. Figure 15 illustrates a GaAs boule which has been ground accurately to diameter with an orientation flat. X-ray topographs of etched test slices reveal that no significant work damage is introduced by the centerless grinding operation. The polished slices shown have a diameter of 1.975 ± 0.001 in.—a thickness of 0.018 in. and a (110) flat. The availability of round oriented (100) substrates fabricated to tight dimensional tolerances and with rounded edges (as in silicon technology today) will have important implications as far as moving towards a truly low-cost, higher yield automated GaAs device processing technology in the future.

Acknowledgements – The authors gratefully acknowledge the advice and encouragement of Dr R. A. Reynolds, (Material Sciences Office, DARPA) and Dr H. C. Nathanson in this work. We are indebted to Dr J. G. Oakes, Dr M. C. Driver and Dr M. Conn (Westinghouse Advanced Technology Laboratories, Baltimore) for their support and for providing the FET performance data quoted in this work. We also wish to thank Dr. W. J. Takei for his contribution in the X-ray topographic studies. The excellent technical assistance of L. J. Wesoloski and W. E. Bing in crystal growth, T. A. Brandis and E. A. Halgas in substrate preparation and P. Kost, D. J. Gustafson and J. C. Neidigh in ion implantation is gratefully acknowledged

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High-Purity Semi-Insulating GaAs Material for Monolithic Microwave Integrated Circuits

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Abstract—Liquid-Encapsulated Czochralski (LEC) growth of large-diameter bulk GaAs crystals from pyrolytic boron nitride (PBN) crucibles has been shown to yield high crystal purity, stable high resistivities, and predictable direct ion-implantation characteristics. Undoped ($\lesssim$low 10^{14} cm^{-3} chromium) and lightly Cr-doped (low 10^{15} cm^{-3} range) (100)-GaAs crystals, synthesized and pulled from PBN crucibles contain residual shallow donor impurities typically in the mid 10^{14} cm^{-3}, exhibit bulk resistivities above 10^{7} $\Omega \cdot$ cm, and maintain the high sheet resistances required for IC fabrication ($>10^{6}$ $\Omega/\square$) after implantation anneal. Direct ^{29}Si channel implants exhibit uniform ($\pm$ 5 percent) and predictable LSS profiles, high donor activation (75 percent), and 4800- to 5000-cm^2/V $\cdot$ s mobility at the (1 to 1.5) $\times$ 10^{17} cm^{-3} peak doping utilized for power FET's.

It has also been established that LEC crystals can provide the large-area, round (100)-substrates which will be required to realize a reproducible, low-breakage GaAs IC processing technology. The fabrication of 2-in-diameter GaAs substrates to tight dimensional tolerances, with (110)-orientation flats and edge rounding has been demonstrated experimentally.

Manuscript received September 8, 1980; revised October 1, 1980. This research was partially supported by the Defense Advanced Research Projects Agency and monitored by the Office of Naval Research under Contract N00014-80C-0445.

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I. Introduction

THE ADVENT of monolithic GaAs IC's is expected to have a broad impact on microwave signal processing and power amplification with impressive advances in the performance and cost-effectiveness of future advanced systems for military radar and telecommunications being anticipated. The present development of monolithic microwave GaAs circuits is based on a selective direct ion implantation of semi-insulating substrates because of its greater flexibility compared with epitaxial techniques for planar device processing. However, direct-implantation technology imposes severe demands on the quality of the semi-insulating GaAs, and the unpredictable and often inferior properties of commercially available Bridgeman and gradient freeze substrates in the past has been a major limitation to at-

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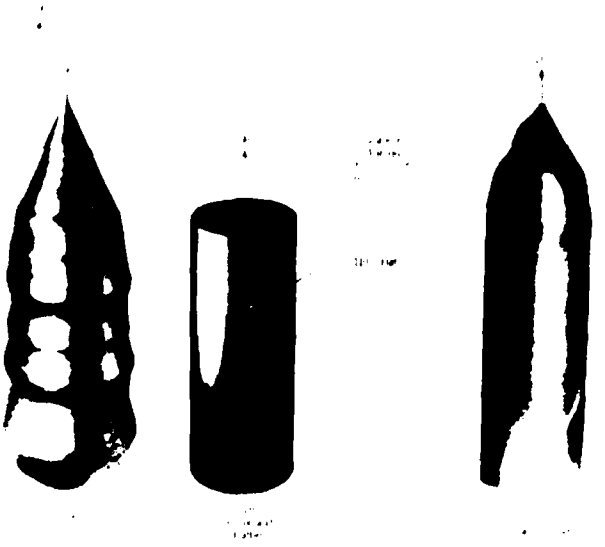
taining uniform and predictable device characteristics by implantation. These problems of substrate reproducibility are now well recognized in a symptomatic sense and are probably associated with excessive and variable concentrations of impurities, particularly silicon and chromium, and with the redistribution of these impurities during implantation and thermal processing. Monolithic GaAs circuits require substrates which 1) exhibit stable, high resistivities during thermal processing, to maintain both good electrical isolation and low parasitic capacitances associated with active elements; 2) contain very low total concentrations of ionized impurities so that the implanted FET channel mobility is not degraded; and 3) permit fabrication of devices of predictable characteristics so that active and passive elements can be matched in monolithic circuit designs.

Another important consideration is the need for uniformly round, large-area substrates. Broad acceptance of GaAs IC's by the systems community will occur only if a reliable GaAs IC manufacturing technology capable of yielding high-performance monolithic circuits at *reasonable costs* is realized. Unfortunately, the characteristic D-shaped slices of boat-grown GaAs material have been a serious deterrent to the achievement of this goal, since much of the standard semiconductor processing equipment developed for the silicon IC industry relies on uniformly round substrate slices. Improvements in the basic GaAs materials and its availability as round, large-area substrates are, therefore, key requirements if a high-yield, low-cost GaAs IC processing technology is to be realized in the near future.

To address these problems, the growth of high-quality large-diameter GaAs crystals by Liquid-Encapsulated Czochralski (LEC) and the fabrication technology for producing cassette-compatible large-area substrates from these circular cross-section crystals has been investigated. The growths were performed in a high-pressure LEC puller, where crystal purity can be preserved by *in situ* elemental compounding [1] and *reproducible* semi-insulating GaAs achieved by employing silicon-free pyrolytic boron nitride crucible techniques [2]-[5]. The growth of 2- and 3-in diameter, (100)-oriented GaAs crystals, investigations of materials purity and semi-insulating properties, and their characterization for directly implanted power IC fabrication are reported here.

II. LEC Crystal Growth and Substrate Preparation

Liquid-Encapsulated Czochralski (LEC) growth was first demonstrated experimentally in 1962 by Metz *et al.* [6] for the growth of volatile PbTe crystals, and has since been developed by Mullin *et al.* [7] for several III-V crystals. In this Czochralski technique, the dissociation of the volatile As from the GaAs melt which is contained in a crucible is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a nonreactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure. *In situ* compound synthesis can be carried out from the elemental Ga and As components since the boric oxide melts before significant sublimation starts to take place (~450°C). Compound synthesis occurs rapidly and exothermally at about 820°C under a sufficient inert gas pressure (~60 atm) to prevent sublimation of the arsenic component. Crystal growth is initiated from the stoichiometric melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.



(a) (b) (c)

Fig. 1. Photograph illustrating: (a) as-grown, nominally 2-in-diameter semi-insulating, (100) GaAs crystal; (b) (100) GaAs crystal centerless ground to 1.975 ± 0.005-in diameter with (110) flat; (c) (111) GaAs crystal grown with $2 \pm \frac{1}{16}$-in diameter utilizing "coracle" method.

The Melbourn high-pressure LEC puller (which is manufactured by Metals Research Ltd., Cambridge, England, and is the outcome of developmental efforts at the Royal Radar and Signals Establishment) is currently being introduced by many laboratories for the growth of large bulk GaAs as well as GaP and InP. The puller consists of a resistance-heated 6-in-diameter crucible system capable of charges up to about 10 kg and can be operated at pressures up to 150 atm. The GaAs melt within the pressure vessel can be viewed by means of a closed-circuit TV system. A high-sensitivity weight cell continuously weighs the crystal during growth and provides a differential weight signal for manual diameter control. In addition, a unique diameter control technique which involves growing the crystal through a diameter-defining aperture made of silicon nitride, has been developed for (111)-oriented growth. In this "coracle" technique, the defining aperture is fabricated from pressed silicon nitride which conveniently floats at the GaAs melt/B_2O_3 encapsulant interface.

In our studies, a reproducible growth methodology for preparing nominally 2- and 3-in-diameter, (100)-oriented GaAs crystals free of major structural defects such as twin planes, lineage, inclusions, and precipitates has been successfully established over the course of about 40 experimental growths. A photograph of a typical 2-in nominal diameter, (100)-semi-insulating GaAs crystal grown from a 3-kg charge is shown in Fig. 1(a). The use of very clean conditions during crucible loading and growth, vacuum baking of the boric oxide encapsulant to assure a water-free oxide, and a growth technique to produce crystals with sharp cone angles [8] during the initial stages of growth were found to be essential ingredients to achieving twin-free (100) growths. The growth of chromium-

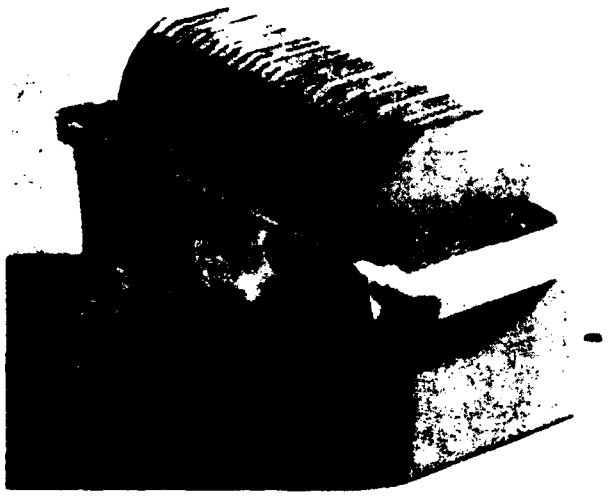


Fig. 2. Photograph of high-purity semi-insulating GaAs wafers sawn on the ⟨100⟩ growth axis from a centerless ground crystal with diameter of 1.975 ± 0.005 in. Wafers have double ⟨110⟩ flats and rounded edges.

free semi-insulating GaAs crystals from melts synthesized *in situ* from 6/9's purity Ga and As charges and contained in a pyrolytic boron nitride crucible has been emphasized in these studies. However, GaAs crystals pulled from undoped and chromium doped melts contained in conventional fused silica crucibles have also been carried out for comparison of materials properties.

Limited experience has also been gained in coracle growths which yield significantly improved diameter uniformity (±1/16 in) as shown in Fig. 1(c). Unfortunately, its utilization is restricted to ⟨111⟩ growths because of severe twinning in ⟨100⟩-coracle growths [9]. However, device fabrication employing ion implantation or epitaxial techniques, is normally carried out on (100)-GaAs surfaces. The coracle technology, therefore, offers little advantage at the present time since the ⟨111⟩-oriented crystals would have to be sliced at a 54° angle and would thus yield elliptical (100) wafers. Our preliminary assessments of the structural quality of ⟨111⟩-oriented LEC crystals grown by the "coracle" method (as determined by X-ray topography and dislocation-etching techniques) indicate that such crystals are often characterized by excessive dislocation-generation and formation of microtwins near the crystal periphery while extensive activation of {111} ⟨110⟩ glide systems occurs in the interior of the crystal. The poor structural quality of the outer regions of coracle-grown ⟨111⟩ crystals often leads to extensive twinning as shown in Fig. 1(c) where a twin boundary can be seen cutting diagonally across the crystal approximately $\frac{2}{3}$ down the axis.

An alternative approach to achieving uniform, circular cross section (100)-oriented GaAs wafers is illustrated in Fig. 1(b), where a ⟨100⟩ ingot has been ground accurately to diameter with a (110) orientation flat by conventional grinding techniques. Surface work damage was removed by etching. Approximately 100 polished wafers of uniform diameter with a thickness of about 0.020 in have been obtained from such crystals. Fig. 2 shows a photograph of a batch of high-purity semi-insulating GaAs wafers sawn on the (100) orientation and fabricated to tight dimensional tolerances (1.975 ± 0.005-in diameter and 0.020 ± 0.001-in thickness), with ⟨110⟩ flats and edge rounded to minimize breakage during handling.

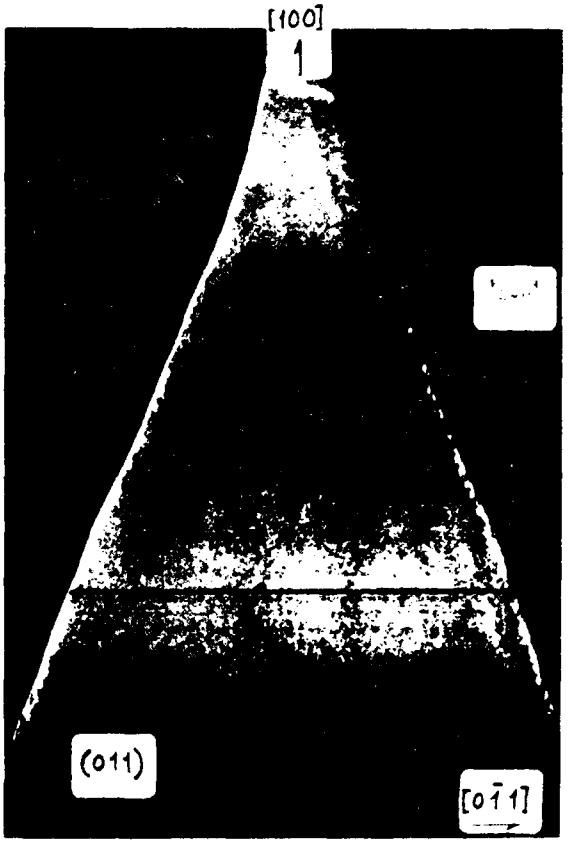


Fig. 3. Reflection X-ray topograph (g = ⟨260⟩) of a (011) longitudinal section cut from a ⟨100⟩ GaAs crystal grown with a cone angle of 27°. Crystal pulled from pyrolytic boron nitride crucible.

III. Characterization

A. Crystalline Perfection

Large-diameter (≤ 3-in) ⟨100⟩ LEC GaAs crystals are usually characterized by radially nonuniform dislocation distributions exhibiting maximum dislocation densities in the 10^4- to 10^5-cm^{-2} range. The dislocation-generation mechanism is thought to be due primarily to thermally induced stresses which, owing to the large convective heat transfer coefficient of the B_2O_3 encapsulating layer and the temperature difference between the crystal interior and the B_2O_3 ambient near the growth interface, can exceed the critical resolved shear stress for dislocation motion [10]. For crystal growths at diameters ~ $\frac{1}{2}$ in, the attendant thermal stresses are diminished, and the crystals can be grown entirely dislocation free [11]. For these small crystals, successful growth free of twins and dislocations depends upon growth conditions which yield proper stoichiometry [12], interface shape [13], [14], and crystal cone angle [8], [15].

Our investigations on improving the structural quality of large-diameter ⟨100⟩ GaAs crystals have concentrated on determining the optimum conditions for initiating a dislocation-free growth and eliminating the tendency toward twinning which has often frustrated ⟨100⟩ GaAs growth efforts in the past. Fig. 3 shows a reflection X-ray topograph of a longitudinal section of the seed-end cone of a ⟨100⟩ GaAs crystal cor-

TABLE I
HIGH-SENSITIVITY SECONDARY ION MASS SPECTROSCOPY ANALYSIS† OF LEC SEMI-INSULATING GaAs CRYSTALS PULLED FROM HIGH-PURITY PYROLITIC BORON NITRIDE CRUCIBLES

Crystal	C*	O*	Si	S	Se	Te	Cr	Mg	Mn	B	Doped Yes	Doped No
BN-1 (s)	2e15	1.5e16	4.8e14	5.7e14	2e13	1e12	< 4e14	1e15	7e14	2.3e15		✓
BN-2 (s)	1e16	6e16	6e14	2e15	1e15	7e13	5.6e14	4e14	8e14	1.7e17		✓
BN-3 (s)	3e15	1.3e16	9.3e14	4.2e14	3e14	< 5e12	4.3e14	2e15	1e15	5.4e17		✓
BN-4 (s)	-	-	2e15	8e14	2e14	1e14	1e16	2.5e15	2e15	1.5e17	Cr	
BN-6 (t)	2.9e15	9.8e15	5.4e14	5e14	9.4e13	< 5e12	5.4e14	2.5e15	1.7e15	6.9e17		✓
BN-8 (s)	1.1e16	3.7e16	8.7e15	1.1e15	5e13	7e12	< 4e14	8.5e14	< 7e14	7.3e16	Si	
BN-10 (s)	2e15	1e16	8.6e14	1.5e15	7e14	7e12	< 4e14	3.6e15	1.2e15	2e18		✓
BN-11 A (s)	4.3e15	1.8e16	6.4e14	1e15	8e13	6e12	6.4e15	3.2e15	1.4e15	1.9e17	Cr	
BN-11 B (s)	3e15	1.3e16	7.6e14	8.7e14	1e14	8e12	6.3e15	4.4e15	1.6e15	1.9e17	Cr	
BN-12 (s)	2e16	7e16	1e15	2e15	5e14	6e13	3.2e15	3e14	8e14	1.8e17	Cr	
BN-13 (s)	-	-	< 3e14	4e15	2e14	1e13	2e15	5e14	7e14	7e16	Cr	
BN-13 (t)	-	-	< 3e14	3e15	5e14	1e13	4e15	8e14	7e14	2e17	Cr	
BN-14 (s)	-	-	4e14	8e14	9e14	8e12	6e14	1e15	8e14	3e17		✓
BN-14 (t)	-	-	7e14	1e15	1e15	1e13	1e15	9e14	1e15	7e17		✓
BN-15 (s)	-	-	< 3e14	1e15	1e14	9e12	3e15	7e14	8e14	7e16	Cr	
BN-15 (t)	-	-	< 3e14	2e15	5e14	2e13	5e15	1e15	8e14	2e17	Cr	
Detection Limit	-	-	3e14	3e14	5e12	5e12	4e14	3e14	7e14	8e12		

† Sims analysis courtesy Charles Evans & Associates, San Mateo CA
(s) Seed end sample
(t) Tang end sample
* Detection limits for C, O, Fe (< mid 10^{15} cm^{-3} not well defined

TABLE II
HIGH-SENSITIVITY SECONDARY ION MASS SPECTROSCOPY ANALYSIS† OF GaAs CRYSTALS GROWN BY LEC AND BOAT-GROWTH METHODS

Crystal	C	O	Si	S	Se	Te	Cr	Mg	Mn	B	Doped Yes	Doped No
LEC/PBN (a)	5e15	2e16	5e14	1e15	4e14	1e13	4e14	7e14	8e14	5e17		✓
LEC/QTZ (b)	6e15	-	1e15	2e15	3e14	4e13	2e16	2e14	8e14	1e15	Cr	
	8e15	4e16	7e14	2e15	3e13	4e13	5e14	3e14	7e14	1e15		✓
	7e15	4e16	9e14	9e14	7e13	3e13	5e14	3e14	6e14	3e15		✓
	5e16	4e16	8e14	1e15	2e14	5e13	1e16	5e14	7e14	2e15	Cr ✓	
	8e16	3e16	2e15	2e15	4e13	2e13	1e16	5e14	8e14	1e15	Cr ✓	
LEC/QTZ (c)	-	-	5e15	6e15	5e14	5e13	2e16	2e15	3e15	2e15	Cr ✓	
	-	-	8e15	4e15	4e14	4e13	6e16	3e15	2e15	2e15	Cr ✓	
	-	-	4e16	4e15	9e14	4e14	1e15	2e15	1e15	1e15		✓
	-	-	2e15	5e15	3e13	7e13	3e16	2e15	1e15	1e15	Cr ✓	
Boat Grown (c)	-	-	8e15	3e15	3e14	2e13	2e16	2e15	1e15	1e14	Cr ✓	
	-	-	6e15	6e15	3e14	2e13	4e16	1e15	1e15	6e14	Cr ✓	
	-	-	2e16	8e15	2e13	4e15	9e16	2e15	2e15	7e14	Cr ✓	
	-	-	5e15	3e15	5e13	5e13	2e16	1e15	2e15	1e15	Cr ✓	

(a) Representative of the Values Shown in Table I
(b) Material Prepared In-House
(c) Material from Commercial Suppliers
† Sims Analysis Courtesy Charles Evans & Assoc., San Mateo, CA.

responding to a cone angle of 27° to the crystal axis. Dislocation-free growth is initiated using a Dash-type seeding [16]. As the cone diameter increases, the regions of highest dislocation density ($<10^3$ cm^{-2}) are confined to the crystal interior and a layer near the crystal surface corresponding to regions of maximum thermal stress; however, severe glide plane activation such as that typically observed in flat-top growths [5] has been eliminated. In addition, a steep cone angle like that shown in Fig. 3 has been found to reduce dramatically the tendency toward twinning which normally accompanies shouldering in flat-top growths of ⟨100⟩ GaAs crystals. A dislocation density maximum of $\sim 10^4$ cm^{-2} is observed in etched substrates corresponding to the full crystal diameter (2- and 3-in diameter).

B. Impurity Content and Electrical Characterization

Secondary ion mass spectrometry (SIMS) bulk analysis[1] of LEC GaAs material pulled from both quartz and pyrolytic boron nitride (PBN) crucibles at our laboratories, as well as commercially supplied large-area boat-grown substrates and LEC GaAs pulled from quartz containers have been carried out. A wide range of impurity species were examined. The SIMS data (Tables I and II) taken together with the resistivity data on corresponding substrates (Table III) show clearly the LEC

[1] The SIMS analyses were performed at Charles Evans and Associates, San Mateo, CA, using a Cameca 1MS-3F ion microanalyzer.

TABLE III
RESISTIVITY MEASUREMENTS ON SUBSTRATES† REPRESENTATIVE OF GaAs CRYSTALS PULLED FROM PYROLITIC BORON NITRIDE AND QUARTZ CRUCIBLES

Chromium Content (cm^{-3})	As-Grown Resistivity (Ω cm)	As-Grown R_s ($\Omega/\square$)	Post Implant Anneal R_s ($\Omega/\square$)
LEC/PBN			
Undoped (5e14)	7e7	1.2e9	1.4e7
	6e7	5.3e9	1.3e7
	4.8e7	4.3e8	9e7
5e15	2e8	1.1e9	4.1e8
	1.7e8	4.0e9	4.5e7
LEC/QTZ			
Undoped (5e14)	3e7 tang	7.7e8	$<10^6$[b]
	9e5	2e7	–
	2.5e3	6.1e4	–
	0.09	–	–
	0.35	–	–
5e16	5.8e8	1e10	1.4e9
	3.9e8	1.2e10	4e9
	5.7e8	1.2e10	7e8

[a] Si_3N_4 Capping and 860°C/15 m Annealing
[b] FETs and monolithic circuits fabricated on these substrates found to exhibit excessive leakage.
† Samples are from near crystal shoulder unless otherwise specified

growths from PBN crucibles yield reproducibly high-purity GaAs substrates exhibiting consistently high, thermally stable semi-insulating behavior. Undoped GaAs crystals pulled from quartz crucibles often exhibit variable and anomalously low as-grown resistivities, while commercially supplied Cr-doped semi-insulating GaAs substrates are characterized by impurity contents which vary from supplier to supplier. The detailed SIMS data for crystals pulled from pyrolytic boron nitride crucibles are shown in Table I. Quantitative estimates of impurity concentrations were obtained by calibration against GaAs samples which had been implanted with known doses of specific impurities. Comparative SIMS results for LEC GaAs pulled from PBN and quartz crucibles and boat-grown substrate material are shown in Table II. For LEC GaAs prepared at our laboratories, residual silicon concentrations in the mid 10^{14}-cm^{-3} range are observed in GaAs/PBN samples and somewhat higher concentrations in crystals pulled from quartz crucibles. Commercially supplied LEC and boat-grown crystals grown in quartz containers exhibit silicon levels which range up to mid 10^{16} cm^{-3}, depending upon growth technique and the substrate supplier. The residual chromium content in undoped LEC GaAs crystals pulled from either PBN or fused silica crucibles is below the detection limit of the SIMS instrument to be in the low 10^{14}-cm^{-3} range. Analyses of LEC-grown crystals pulled from Cr-doped melts contained in quartz crucibles reveal that the Cr content (typically 2×10^{16} cm^{-3} at the seed end and approaching 10^{17} cm^{-3} at the tang end) is close to the anticipated doping level based on the amount of Cr dopant added to the melt and its reported segregation behavior [17]. Cr dopant levels of (2 to 9) $\times 10^{16}$ cm^{-3} were observed in material grown by horizontal gradient freeze or Bridgeman methods. The reduced concentration of shallow donor impurities in growths from PBN crucibles permits lower Cr doping levels to be utilized as shown in Table I (BN-11, 12, 13, 15) where typical Cr dopant concentrations range from 3×10^{15} cm^{-3} at the crystal seed end to 6×10^{15} cm^{-3} near the crystal tang end. The corresponding resistivity levels measured in lightly Cr doped ($<5 \times 10^{15}$ cm^{-3}) GaAs/PBN material (Table III) approach those typically observed in heavily Cr doped ($>1 \times 10^{16}$ cm^{-3}) GaAs pulled from fused silica containers. The SIMS studies also indicate that LEC growths from PBN crucibles generally result in high boron concentrations (10^{17}-cm^{-3} range) in the GaAs/PBN material versus low 10^{15}-cm^{-3} concentrations in quartz crucible growth. The results reported in Section IV suggest that boron in GaAs/PBN substrates does not contribute significantly to ionized impurity scattering and remains electrically neutral through implantation processing [18]. No significant differences in carbon ($\sim 10^{16}$ cm^{-3}), oxygen (10^{16} cm^{-3}), selenium (mid 10^{14} cm^{-3}), tellurium ($<10^{14}$ cm^{-3}), and iron (mid 10^{15} cm^{-3}) contents of different GaAs samples are revealed by these investigations; however, the results for carbon and oxygen must be viewed as tentative since detection limits for these elements are not as yet well defined for the SIMS technique.

Resistivity and thermal stability measurements have been carried out on LEC-grown GaAs substrates to determine the suitability of the substrates for ion implantation studies. Table III shows the results of resistivity measurements on substrates representative of GaAs crystals pulled from pyrolytic boron nitride crucibles and, for comparison, quartz crucibles. The substrates were taken from near the crystal shoulder unless indicated otherwise. Substrate resistivities in the mid 10^8-$\Omega \cdot$ cm range are observed in conventionally Cr-doped substrate material (containing mid 10^{16} cm^{-3} Cr concentrations) pulled from quartz crucibles compared to resistivities of mid 10^7 $\Omega \cdot$ cm in undoped GaAs/PBN crystals ($<5 \times 10^{14}$-cm^{-3} Cr content) and resistivities of 10^8 $\Omega \cdot$ cm observed in lightly Cr-doped GaAs/-PBN crystals (mid 10^{15}-cm^{-3} Cr content). In contrast to other work [19], undoped GaAs crystals pulled in our laboratories from fused silica crucibles show lower resistivities and exhibit large seed to tang variations from crystal to crystal, ranging from 10^6 to 10^7 $\Omega \cdot$ cm in one to resistivities as low as 0.09-$\Omega \cdot$ cm range in another crystal, even though the crystals exhibit SIMS impurity concentrations roughly equivalent to those observed in GaAs pulled from pyrolytic boron nitride crucibles.

Thermal stability of substrates for ion implantation was assessed by means of resistivity measurements following an encapsulated anneal of the semi-insulating slice (prior to implantation) to determine whether any conducting surface layers formed as a result of thermal treatment. Samples for the unimplanted, encapsulated anneal test were prepared using the same plasma-enhanced silicon nitride capping process as is used for implantation (see Section IV). The encapsulated wafers were annealed at 860°C for 15 min in a forming gas atmosphere. Surface sheet resistances exceeding 10^6 $\Omega/\square$ are desired after annealing to ensure isolation of passive, as well as active elements in analog IC processing.

Typical sheet resistance data for semi-insulating undoped and lightly Cr-doped ($<5 \times 10^{15}$ cm^{-3}) GaAs/PBN substrates as well as undoped and conventionally Cr-doped ($>1 \times 10^{16}$ cm^{-3}) GaAs substrates before and after encapsulated anneals are shown in Table III. Some degradation in the sheet resistance was always observed as a result of the thermal treatment, but the leakage currents measured in the low-field measurements (10^3 V/cm) and the RF losses observed in monolithic circuits fabricated on these substrates were low. In particular, surface leakages of <30 μA at 15-V bias and high breakdown voltages

of 25 V were measured in interdigitated capacitor structures (5-μm separation and 13.2-mm periphery) to test the performance under the high operating fields normally utilized in monolithic circuits [20]. Additional assessment of the substrate quality was provided by measurements of transport properties of n-doped layers formed by direct ion implantation into the semi-insulating substrates and is discussed in the following section.

IV. Ion Implantation

A direct ion-implantation technology yielding uniform and reproducible doping characteristics across each substrate and from substrate to substrate is highly desired for GaAs IC processing. Our approach implicitly assumes that higher purity semi-insulating GaAs substrates are required to avoid some of the difficulties encountered in the past such as: spurious activation of residual impurities, redistribution phenomena, and interactions with the implanted species. Silicon implantation of undoped LEC GaAs/PBN has, therefore, been emphasized with data from Cr-doped LEC GaAs included for comparison. The characterization of implanted substrates involves diagnostic techniques which are modified to meet the particular requirements of monolithic power amplifier development. Knowledge of the undepleted net carrier concentration per unit area of implanted layers is needed since this quantity will determine both the full channel current and the gate-drain breakdown voltage of gate-recessed power FET's fabricated on the layer [21], [22]. Although output power per unit periphery *may be only weakly dependent on this quantity*, reproducible matching to the passive output tuning circuit should be critically dependent upon it. Attention is then focused on carrier concentration per unit volume since this affects matching to passive input, interstage tuning circuits, and the gain. The pinch-off voltage and its uniformity are not considered directly.

Wafers for implantation are nominally 2-in diameter, cut on the ⟨100⟩ crystal growth axis, and bromine-methanol front surface polished to a thickness of approximately 0.020 in. Partial wafers, but more than $1\frac{1}{4}$ in in greatest dimension, were used for almost all of the tests described here. A 900-Å Si_3N_4 front surface encapsulation is deposited immediately following cleaning (to remove bromine and carbon contamination) and etch-back. This sequence implies that implantation through the Si_3N_4 encapsulant is found to be necessary to ensure a clean Si_3N_4/GaAs interface. Plasma-enhanced reaction of SiH_4 and N_2 at 340°C is used to deposit the Si_3N_4 at a rate of 70 Å/min. Uniformity of Si_3N_4 thickness is ±3 percent while the refractive index is 1.96 ± 1 percent. Implantation is performed at ambient temperature and 7° off normal incidence using the 3-in-diameter cassette-load end station of a 400-kV Varion Extrion implanter. All of the implantations discussed here employed $^{29}Si^+$ generated from an SiF_4 source. The initial choice of Si as the primary implant species was made on the basis of achievable range [23], integrity of the implanted profile through annealing [24], and ability to activate ambient temperature implants [25]. The test implants described here were performed at either 100, 200, and 400 kV or at a pair of lower energies such as 125 and 275 kV to approximate a flat ^{29}Si concentration; recoil implantation from the encapsulant was not considered in calculating doses. 2500 Å of 7-percent phosphosilicate glass was deposited on both surfaces prior to annealing. The implanted samples were annealed at 860°C for 15 min in flowing forming gas. Both the heating and cooling cycles were controlled.

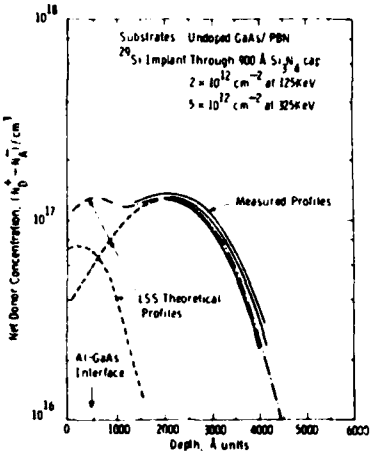


Fig. 4. Uniformity of implant profiles in undoped GaAs/PBN substrates measured by *C–V* profiling.

A. Implant Profiles and Activation

Fig. 4 shows the net donor profiles achieved by $^{29}Si^+$ implantation into undoped GaAs/PBN substrates. The data obtained by surface Al Schottky-barrier diodes are representative of variations across each slice and slice-to-slice from approximately $\frac{2}{3}$ of one crystal. The superimposed theoretical curves are generated from tabulated joined half-Gaussian tables [23]. The standard deviations are modified by $\sigma_i^2 \rightarrow \sigma_i^2 + 3 \times 10^{-11}$ cm^2 which may reflect a diffusion process. The stopping power of the encapsulant is assumed equal to that of GaAs and recoil implantation from encapsulant is ignored. The theoretical curves have been scaled in concentration to reflect an activation efficiency of 75 percent.

A more detailed model of the form

$$n(z) = \eta \sum_{E_i} n_I(z, E_i) - N_{A0} \tag{1}$$

provides a better representation of the profiles that is also consistent with Hall data. Equation (1) assumes that the carrier concentration $n(z)$ can be represented by a constant activation efficiency η times the superposition of the implanted Si profiles $n_I(z, E_i)$ less a uniform concentration N_{A0} representing the density of levels that must be filled to raise the Fermi level from its position in the as-grown material to the neighborhood of the conduction band edge. Hall data for the undoped GaAs/PBN samples yield $\eta = 0.72$ and $N_{A0} = 1 \times 10^{16}$/cm^3, compared with Cr-doped GaAs substrates which yield $\eta \simeq 0.85$ and $N_{A0} \simeq 4 \times 10^{16}$/cm^3. It should be reiterated that these samples remain n-type semi-insulating through unimplanted, encapsulated anneals; N_{A0}^- may, in fact, be the density of deep donors ionized as a result of the acceptor concentration exceeding the residual shallow donor concentration.

Surface Hall-effect measurements yield a net donor concen-

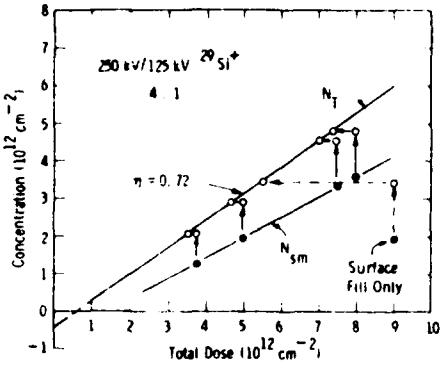


Fig. 5. Activation efficiency by Hall measurements of ^{29}Si implants in undoped GaAs/PBN substrates. The data as measured (N_{sm}) and after correction for surface depletion and implant deposition in nitride cap (N_T) are shown.

tration per unit area

$$Q_u/q = (N_D^+ - N_A^-) = \left\{\int_{\lambda_d}^{\infty} \mu(z)n(z)\,dz\right\}^2 \Big/ \int_{\lambda_d}^{\infty} \mu^2(z)n(z)\,dz \qquad (2)$$

where λ_d is the same surface depletion depth that determines undepleted charge Q_u in actual FET structures. The measured Q_u is potentially modified by depth-dependent Hall and drift mobilities, as well as the Hall factor itself. Both effects are neglected here. This approach is justified by the observation that the saturation current of FET structures prior to gate recess can be represented by

$$I = (1.18 \pm 0.1 \times 10^7 \text{ cm/s})Q_u \qquad (3)$$

(where I has units of amperes per centimeters gate width) independent of concentration level (0.6–1.8×10^{17}/cm^3), type of semi-insulating substrate, activation efficiency achieved, and Hall mobility observed. The saturation velocity noted in (3) may imply a systematic underestimate of the actual Q_u, as a result of the Hall-effect measurement technique [21].

Fig. 5 illustrates the activation data achieved from an undoped GaAs/PBN crystal by Hall measurements. In this case, a fairly extensive series of samples was implanted at a fixed pair of energies and fixed surface/channel dose ratio to yield approximately flat Si profiles at different concentrations. The total dose required at this energy to achieve a specified undepleted concentration can be interpolated directly from the raw data. Corrections are required to obtain η and N_{A0}. An *a priori* correction for surface depletion can be achieved if it is assumed that the net donor concentration profile is flat between the Si_3N_4–GaAs interface and the range of maximum concentration (R_M) of the channel implant; the equivalent, uniform concentration implant depth ($R_M + \sqrt{(\pi/2)}\,\sigma_d$) is known; and the surface depletion barrier is known. For the undoped substrates, the profile is approximately flat; the equivalent depth can be approximated by (11.4) E angstroms, where E is the channel implant energy in kiloelectronvolts, and the surface depletion barrier can be taken to equal 0.6 eV. The vertical arrows in Fig. 5 indicate these corrections to yield total net donor concentration cm^{-2}. The horizontal arrows correct the total implanted Si concentration for 40 percent deposition of the surface fill implant into the Si_3N_4 rather than the GaAs. The slope of the corrected data is the activation efficiency η = 0.72 while the intercept on the vertical axis scaled by the effective depth yields $N_{A0} = 0.9 \times 10^{16}$ cm^{-3}. Direct C-V measurement of these samples yields volume concentrations which agree within ±5 percent of those implied by the corrected Hall data and effective depth agreement ±3 percent. The significance of η and N_{A0} to the ion-implantation technology is that they can be employed in an inverse process to predict undepleted charge and net volume carrier concentration at other channel implant energies and down to volume concentrations as low as 1.2×10^{16}/cm^3. (Prediction at net carrier concentrations in excess of 2×10^{17}/cm^3 is complicated by a concentration dependent activation efficiency.) An even more significant tentative result is that the undoped LEC GaAs/PBN can be consistently grown to yield $\eta = 0.75 \pm 0.03$ and $N_{A0} = 1.0 \pm 0.3 \times 10^{16}$/cm^3.

Comparable data have been assembled for high Cr (0.6–1.2×10^{17} cm^{-3}) LEC GaAs crystals grown from fused silica crucibles and low Cr (3–6×10^{15} cm^{-3}) LEC GaAs grown from pyrolytic boron nitride. Analysis of the high Cr material is complicated by a depth-dependent activation efficiency which is presumably related to Cr pileup near the Si_3N_4–GaAs interface and by thickness variations in the conducting layer owing to compensating Cr in the substrate. For net donor concentrations less than 2×10^{17} cm^{-3} the channel implant activation efficiency $\eta = 0.90 \pm 0.05$ and $N_{A0} = (4$–$8) \times 10^{16}$/cm^3. The low Cr material can be analyzed by the technique described above to yield $\eta = 0.82 \pm 0.06$ and $N_{A0} = (1$–$2) \times 10^{16}$/cm^3, but the behavior at low implanted Si concentrations [$(0.2$–$6) \times 10^{16}$/cm^3)] suggests a possible Si–Cr interaction.

B. Channel Mobility

The ambient temperature surface Hall mobility of FET channel layers ($n = 1.2 \times 10^{17}$/cm^3) implanted into undoped LEC GaAs/PBN is found to be 4900 ± 100 cm^2/V · s. Values of 4300–4600 cm^2/V · s can also be achieved in selected Cr-doped LEC GaAs crystals however. Analysis of this mobility over a broad range of net donor densities reveals significant differences in the behavior of these two types of material as is shown in Fig. 6. The data shown here correspond to the mobility average

$$\mu = \int_{\lambda_d}^{\infty} \mu^2(z)n(z)\,dz \Big/ \int_{\lambda_d}^{\infty} \mu(z)n(z)\,dz \qquad (4)$$

where each point corresponds to a separate sample prepared to yield an approximately flat $n(z)$ profile. The data on undoped samples were obtained from three separate test implant runs and include data from two different crystals. At the lower end of the implanted Si concentration range (1.7×10^{16}–1.5×10^{18} cm^{-3}), the surface depletion depth is so large that an appreciable fraction of the measured carriers for those 100-, 200-, plus 400-kV implants is associated with the half-Gaussian lying beyond R_M. If the undepleted profile were exactly half-Gaussian and $\mu(z)$ could be approximated as a linear function of $n(z)$ only, μ should more properly be associated with $n(R_M)/\sqrt{2}$.

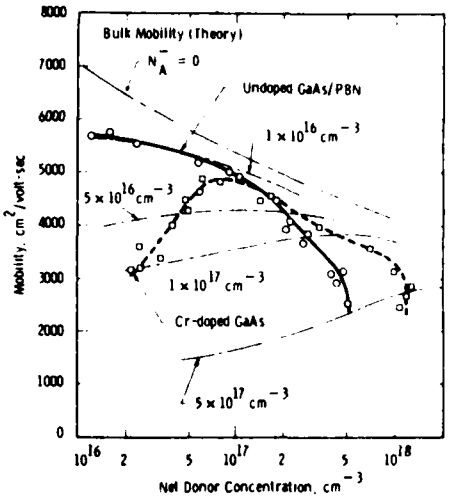


Fig. 6. Measured direct ^{29}Si implant mobility in semi-insulating undoped and Cr-doped GaAs compared with theoretical bulk mobility.

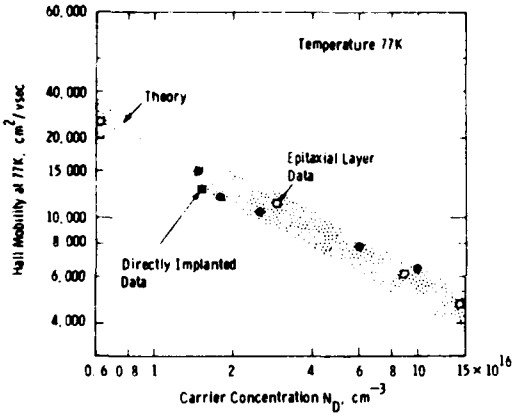


Fig. 7. Directly implanted channel mobility at 77 K in undoped GaAs substrates.

Since this ambiguity is significant only at the lowest concentrations where μ is a weak function of $n(R_M)$, all μ values are plotted at $n(R_M)$. Substrate and process control is demonstrated by implantations designed for $n(R_M) = 1.6 \times 10^{16}$ cm^{-3} reproducibly yielding $n(R_M) = 1.6 \times 10^{16} \pm 0.4 \times 10^{16}$ cm^{-3} with mobilities of 5300-5700 cm^2/V · s. The mobilities of these layers at 77 K are 12 000-14 500 cm^2/V · s (see Fig. 7). These results are believed to be significant improvements over previously reported work.

The experimental data shown in Fig. 6 are overlaid by theoretical bulk drift mobility data drawn from tables published by Walukiewicz *et al.* [26]. Although comparison of depth averaged Hall-mobility data with this theory may not be strictly valid, this approach is believed to provide a valuable engineering perspective. Fig. 6 shows that the observed channel mobilities in undoped GaAs/PBN substrates are consistent with the presence of a compensating acceptor density of about 1×10^{16} cm^{-3} in agreement with the value derived from activation measurements. At net donor concentrations greater than $(1.5\text{-}2) \times 10^{17}$ cm^{-3}, the mobility is observed to decrease rapidly implying an increase in the net acceptor density. The observed decrease in mobility strongly suggests that an increasing fraction of the implanted ^{29}Si resides on acceptor sites such as Si_{As}^- or $Si_{Ga}V_{Ga}^-$. Similar "amphoteric" behavior has been documented for both Group IV and Group VI impurities in high-purity VPE growth [27]. Detailed mobility analysis [28] indicates that, provided Si acceptor formation during implantation is taken into account, the total activation of electrically active $N_D + N_A$ centers (above the residual background acceptor density of about 1×10^{16} cm^{-3}) is always 100 percent. This result suggests the absence of inactive ^{29}Si due to processes such as interstitial or pair formation, spurious activation of other impurities or the generation of active native defects, and that the net donor activation efficiency is determined by thermodynamic considerations.

Hall mobility of Cr-doped GaAs/silica (>5×10^{16} cm^{-3} Cr) exhibits strikingly different characteristics. The data were obtained from three different crystals to ensure representative behavior. Net doping saturation which occurs at about 2×10^{18} cm^{-3} is displaced to higher levels with increasing Cr content. At low carrier concentration levels (10^{16}-cm^{-3} range), anomalously low mobility values are observed in implanted Cr-doped GaAs and the observed mobility appears to be strongly dependent on the Cr content. Reproducibility at carrier concentrations below about 5×10^{16} cm^{-3} is very poor. Preliminary measurements of implanted channels formed in light Cr-doped GaAs/PBN substrates (~5×10^{15}-cm^{-3} Cr content) indicate mobilities which lie midway between the undoped GaAs/PBN and the Cr-doped GaAs/silica curves shown in Fig. 6. A self-consistent analysis of the mobility and activation of Cr-doped GaAs leads to the conclusions that formation of Cr-Si complexes and Cr control of the formation of silicon acceptors are important phenomena [29].

V. Conclusions

Significant progress has been made towards developing large-diameter semi-insulating GaAs crystals of improved quality by LEC growth for direct-ion implantation. The intent has been to establish a source of reproducibly high-quality GaAs substrates for analog power IC development [30] by achieving 1) thermally stable, semi-insulating properties without resorting to intentional Cr doping (or at least to reduce the Cr content significantly) to avoid the serious redistribution problems associated with this impurity [31], [32], 2) uniform and predictable doping characteristics by direct ^{29}Si implantation, and 3) demonstrating that uniform, round cross-section slices suitable for low-cost IC processing can be fabricated from LEC crystals.

The use of *in situ* compounding, PBN crucible techniques, and very low moisture content B_2O_3 (assured by vacuum baking) appear to be the key ingredients to achieving *reproducible* semi-insulating ⟨100⟩ crystals of high purity and structural quality. Quantitative SIMS analyses indicate that residual silicon, Group VI impurities, and chromium can be maintained below the 10^{15}-cm^{-3} range in undoped GaAs crystals pulled from both PBN and quartz containers [19]. However, *consistent* high resistivities (>10^7 Ω · cm) and thermally annealed sheet resistances (>10^6 Ω/□), which yield acceptably low leakages and RF losses in analog circuits, are achieved from only GaAs/PBN

grown crystals and not, in contrast to other studies [19], from GaAs crystals pulled from quartz crucibles.

Direct ion-implantation studies of undoped and lightly Cr doped (low 10^{15}-cm^{-3} Cr content) using ^{29}Si implants yield reproducible implant profiles, showing excellent agreement with LSS theoretical predictions. Directly implanted channels with the (1 to 1.5) × 10^{17}-cm^{-3} peak donor concentrations required for X-band power FET structures yield electron mobilities between 4800 and 5000 cm^2/V · s. A compensating acceptor density of 1 × 10^{16} cm^{-3} or less is observed in undoped GaAs/PBN substrates compared with up to 10^{17}-cm^{-3} levels in conventional Cr-doped GaAs. Channel dopings down to 2 × 10^{16} cm^{-3} have been implanted in undoped GaAs/PBN substrates and mobilities of 5700 at 298 K and 14 500 cm^2/V · s at 77 K have been measured. Strong amphoteric doping behavior is observed at silicon implant concentrations approaching 10^{18} cm^{-3} and the total electrical activation, $N_D + N_A$, is 100 percent.

Monolithic analog amplifier circuits fabricated on high-purity semi-insulating LEC GaAs substrates (and reported in the companion paper appearing in this Special Issue [30]) have resulted in RF output powers approaching 1 W at associated 5-dB gain with octave bandwidth at X-band frequencies.

The materials preparative techniques commonly used in the silicon industry have been applied successfully to bulk LEC crystals to demonstrate the fabrication of uniformly round, large-area (100)-GaAs wafers, which will be needed to realize a reliable, low-cost GaAs IC manufacturing technology.

Acknowledgment

The authors wish to thank Dr. H. C. Nathanson for his advice and encouragement in this work. They are indebted to Dr. J. G. Oakes, Dr. M. C. Driver, and Dr. M. Cohn (Westinghouse Advanced Technology Laboratories, Baltimore, MD) for their support and for providing the FET performance data quoted in this work. They also wish to thank Dr. T. T. Braggins for electrical and transport measurements, and Dr. W. J. Takei for his contribution in the X-ray topographic studies. The excellent technical assistance of L. L. Wesoloski and W. E. Bing in crystal growth, T. A. Brandis in substrate preparation, and P. Kost, D. J. Gustafson and J. C. Neidigh in ion implantation is gratefully acknowledged.

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